

GPU: 8800GT - G92-270-A2  
MEM:512M 8x 16MX32-HYNIX H5RS5223CFR  
NVVDD:CHL8228-IR3598-DIRECT\_FET  
FBVDD:CHL8228-IRF3598-DIRECT\_FET

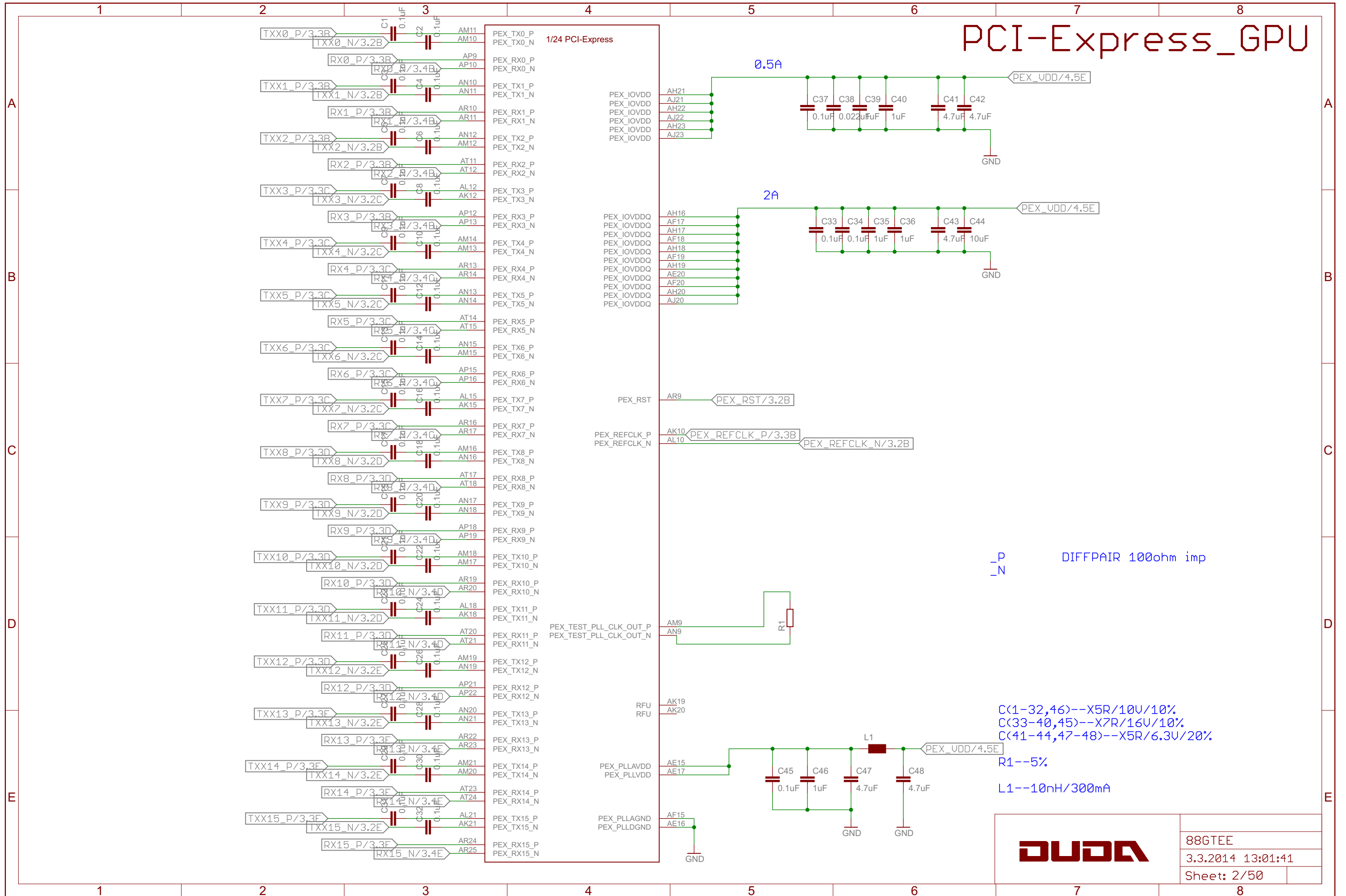
mem impedance 40ohm  
vga signals 75ohm  
diffpairs 100ohm

TIMELINE

9.2.2014--Initial concept  
10.2.2014--CORE/MEM symbol+package,PCI-E  
11.2.2014--Frame Buffer A/B/C/D  
13.2.2014--FBA mem/NVVDD  
14.2.2014--FBB/FBC/FBD  
16.2.2014--IFPAB/IFPCD  
20.2.2014--DACA/DACC/MIOA/MIOB  
22.2.2014--POWER\_I  
2.3.2014--POWER\_II



88GTEE
3.3.2014 13:01:41
Sheet: 1/50



# PCI-Express\_GPU

1/24 PCI-Express

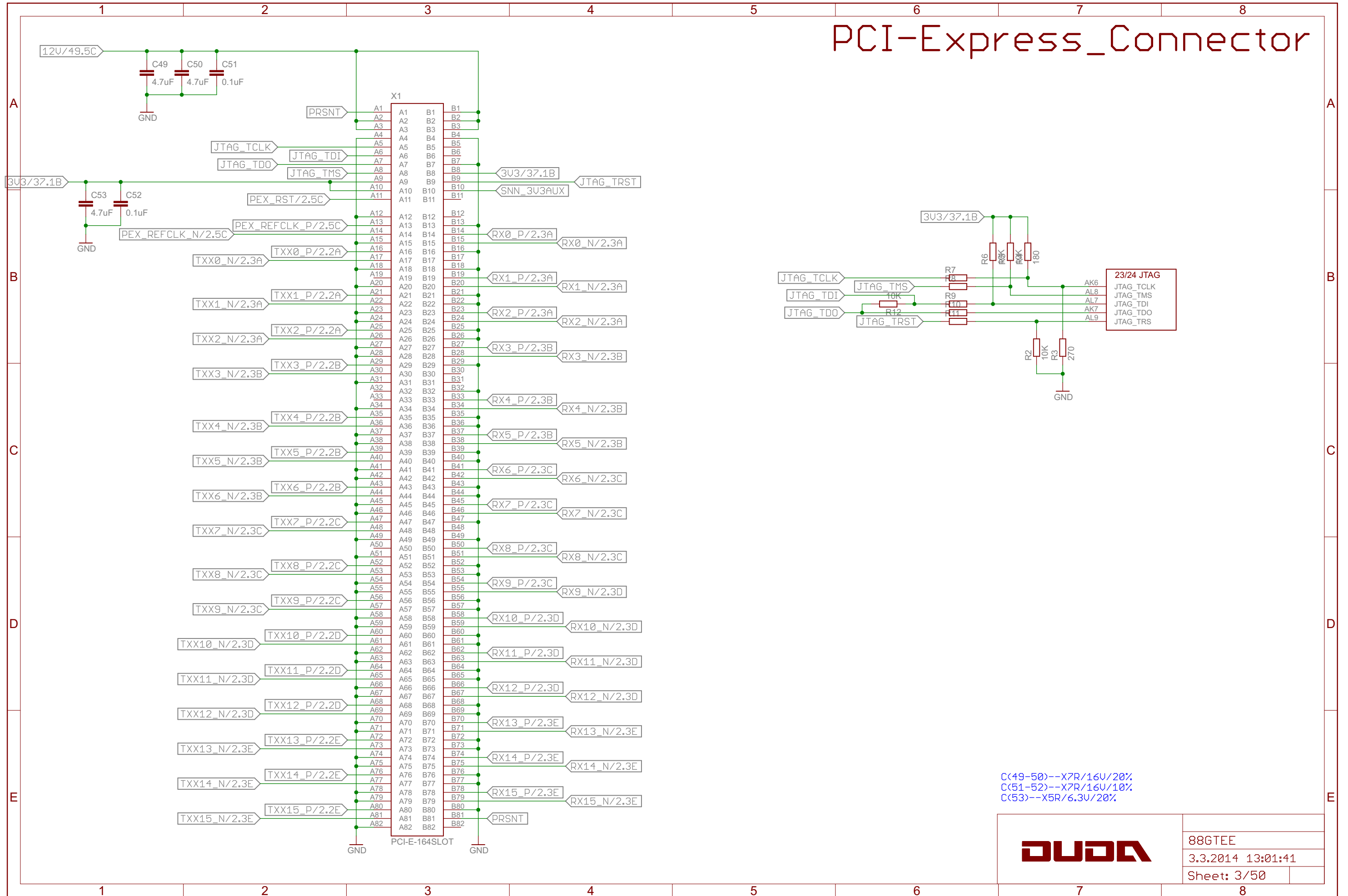
\_P  
\_N DIFFPAIR 100ohm imp

C(1-32,46)--X5R/10V/10%  
 C(33-40,45)--X7R/16V/10%  
 C(41-44,47-48)--X5R/6.3V/20%  
 R1--5%  
 L1--10nH/300mA



88GTEE
3.3.2014 13:01:41
Sheet: 2/50

# PCI-Express\_Connector



C(49-50)--X7R/16V/20%  
 C(51-52)--X7R/16V/10%  
 C(53)--X5R/6.3V/20%

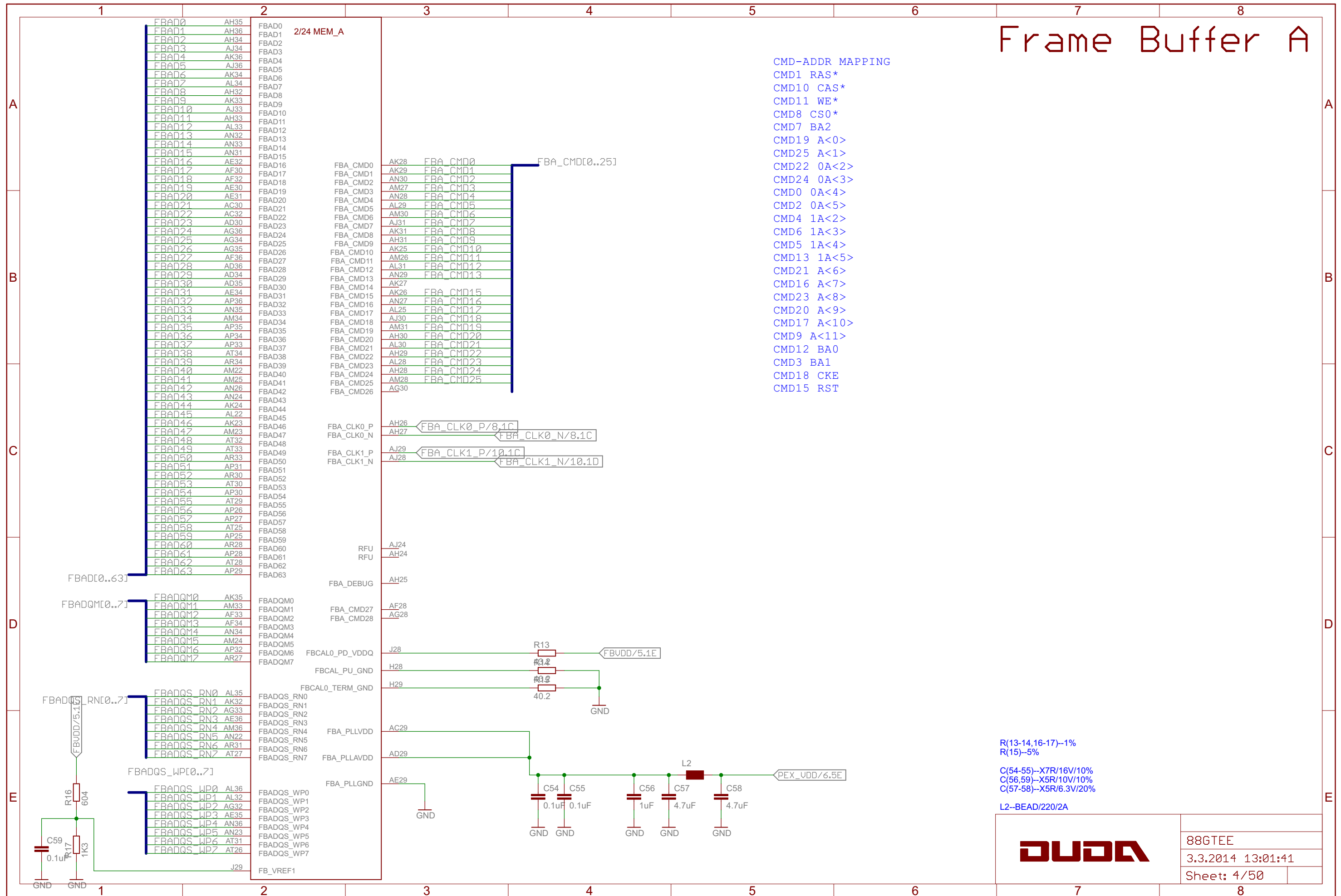


88GTEE  
 3.3.2014 13:01:41  
 Sheet: 3/50

# Frame Buffer A

## CMD-ADDR MAPPING

- CMD1 RAS\*
- CMD10 CAS\*
- CMD11 WE\*
- CMD8 CS0\*
- CMD7 BA2
- CMD19 A<0>
- CMD25 A<1>
- CMD22 0A<2>
- CMD24 0A<3>
- CMD0 0A<4>
- CMD2 0A<5>
- CMD4 1A<2>
- CMD6 1A<3>
- CMD5 1A<4>
- CMD13 1A<5>
- CMD21 A<6>
- CMD16 A<7>
- CMD23 A<8>
- CMD20 A<9>
- CMD17 A<10>
- CMD9 A<11>
- CMD12 BA0
- CMD3 BA1
- CMD18 CKE
- CMD15 RST



2/24 MEM\_A

FBA_CMD0	AK28	FBA_CMD0	FBA_CMD[0..25]
FBA_CMD1	AK29	FBA_CMD1	
FBA_CMD2	AN30	FBA_CMD2	
FBA_CMD3	AM27	FBA_CMD3	
FBA_CMD4	AN28	FBA_CMD4	
FBA_CMD5	AL29	FBA_CMD5	
FBA_CMD6	AM30	FBA_CMD6	
FBA_CMD7	AJ31	FBA_CMD7	
FBA_CMD8	AK31	FBA_CMD8	
FBA_CMD9	AH31	FBA_CMD9	
FBA_CMD10	AK25	FBA_CMD10	
FBA_CMD11	AM26	FBA_CMD11	
FBA_CMD12	AL31	FBA_CMD12	
FBA_CMD13	AN29	FBA_CMD13	
FBA_CMD14	AK27		
FBA_CMD15	AK26	FBA_CMD15	
FBA_CMD16	AN27	FBA_CMD16	
FBA_CMD17	AL25	FBA_CMD17	
FBA_CMD18	AJ30	FBA_CMD18	
FBA_CMD19	AM31	FBA_CMD19	
FBA_CMD20	AH30	FBA_CMD20	
FBA_CMD21	AL30	FBA_CMD21	
FBA_CMD22	AH29	FBA_CMD22	
FBA_CMD23	AL28	FBA_CMD23	
FBA_CMD24	AH28	FBA_CMD24	
FBA_CMD25	AM28	FBA_CMD25	
FBA_CMD26	AG30		

FBA_CLK0_P	AH26	FBA_CLK0_P/8.1C
FBA_CLK0_N	AH27	FBA_CLK0_N/8.1C
FBA_CLK1_P	AJ29	FBA_CLK1_P/10.1C
FBA_CLK1_N	AJ28	FBA_CLK1_N/10.1D

RFU	AJ24	
RFU	AH24	

FBA_DEBUG	AH25	
FBA_CMD27	AF28	
FBA_CMD28	AG28	

FBCAL0_PD_VDDQ	J28	R13	FBUDD/5.1E
FBCAL0_PU_GND	H28	R14	
FBCAL0_TERM_GND	H29	R15	40.2

FBA_PLLVDD	AC29		
FBA_PLLAVDD	AD29		
FBA_PLLGND	AE29		

FBCAL0_PD_VDDQ	J28		
----------------	-----	--	--

FB_VREF1	J29		
----------	-----	--	--

R(13-14,16-17)--1%  
R(15)--5%  
C(54-55)--X7R/16V/10%  
C(56,59)--X5R/10V/10%  
C(57-58)--X5R/6.3V/20%  
L2--BEAD/220/2A

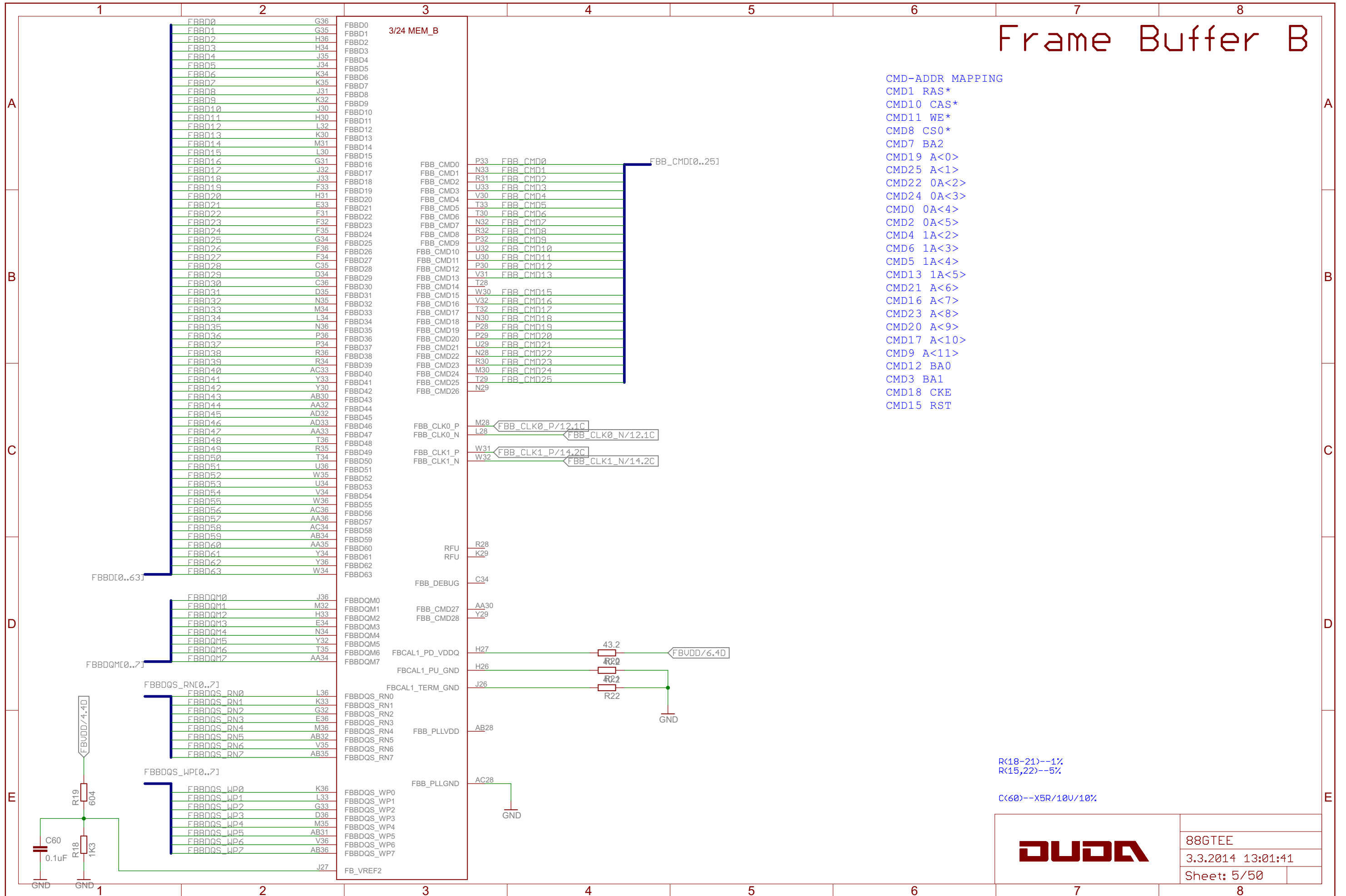


88GTEE
3.3.2014 13:01:41
Sheet: 4/50

# Frame Buffer B

## CMD-ADDR MAPPING

- CMD1 RAS\*
- CMD10 CAS\*
- CMD11 WE\*
- CMD8 CS0\*
- CMD7 BA2
- CMD19 A<0>
- CMD25 A<1>
- CMD22 0A<2>
- CMD24 0A<3>
- CMD0 0A<4>
- CMD2 0A<5>
- CMD4 1A<2>
- CMD6 1A<3>
- CMD5 1A<4>
- CMD13 1A<5>
- CMD21 A<6>
- CMD16 A<7>
- CMD23 A<8>
- CMD20 A<9>
- CMD17 A<10>
- CMD9 A<11>
- CMD12 BA0
- CMD3 BA1
- CMD18 CKE
- CMD15 RST



R(18-21)--1%  
R(15,22)--5%  
C(60)--X5R/10V/10%

	88GTEE
	3.3.2014 13:01:41
	Sheet: 5/50

# Frame Buffer C

## CMD-ADDR MAPPING

CMD1 RAS\*  
 CMD10 CAS\*  
 CMD11 WE\*  
 CMD8 CS0\*  
 CMD7 BA2  
 CMD19 A<0>  
 CMD25 A<1>  
 CMD22 0A<2>  
 CMD24 0A<3>  
 CMD0 0A<4>  
 CMD2 0A<5>  
 CMD4 1A<2>  
 CMD6 1A<3>  
 CMD5 1A<4>  
 CMD13 1A<5>  
 CMD21 A<6>  
 CMD16 A<7>  
 CMD23 A<8>  
 CMD20 A<9>  
 CMD17 A<10>  
 CMD9 A<11>  
 CMD12 BA0  
 CMD3 BA1  
 CMD18 CKE  
 CMD15 RST

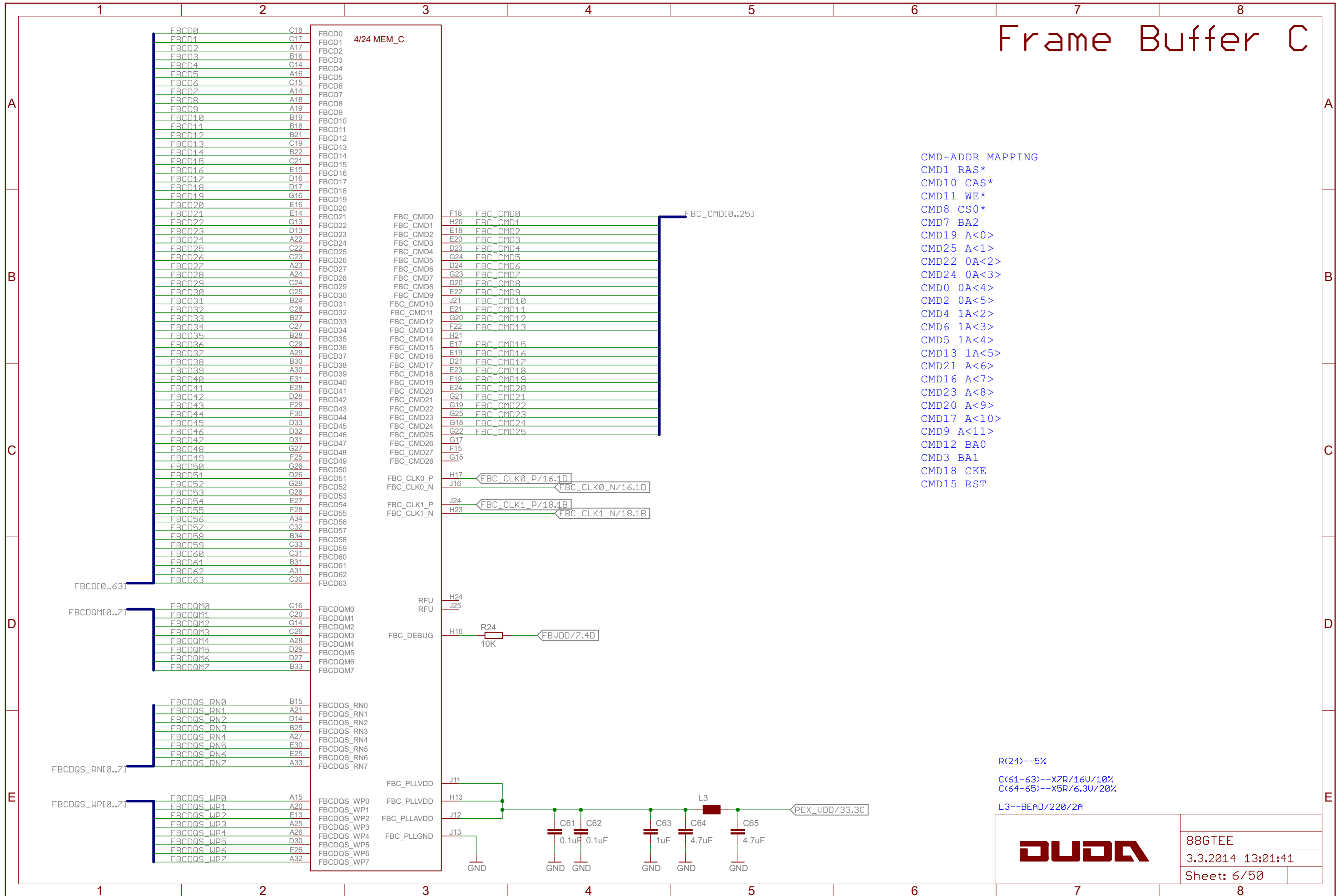
R(24)--5%

C(61-63)--X7R/16U/10%  
 C(64-65)--X5R/6.3U/20%

L3--BEAD/220/2A



88GTEE  
 3.3.2014 13:01:41  
 Sheet: 6/50

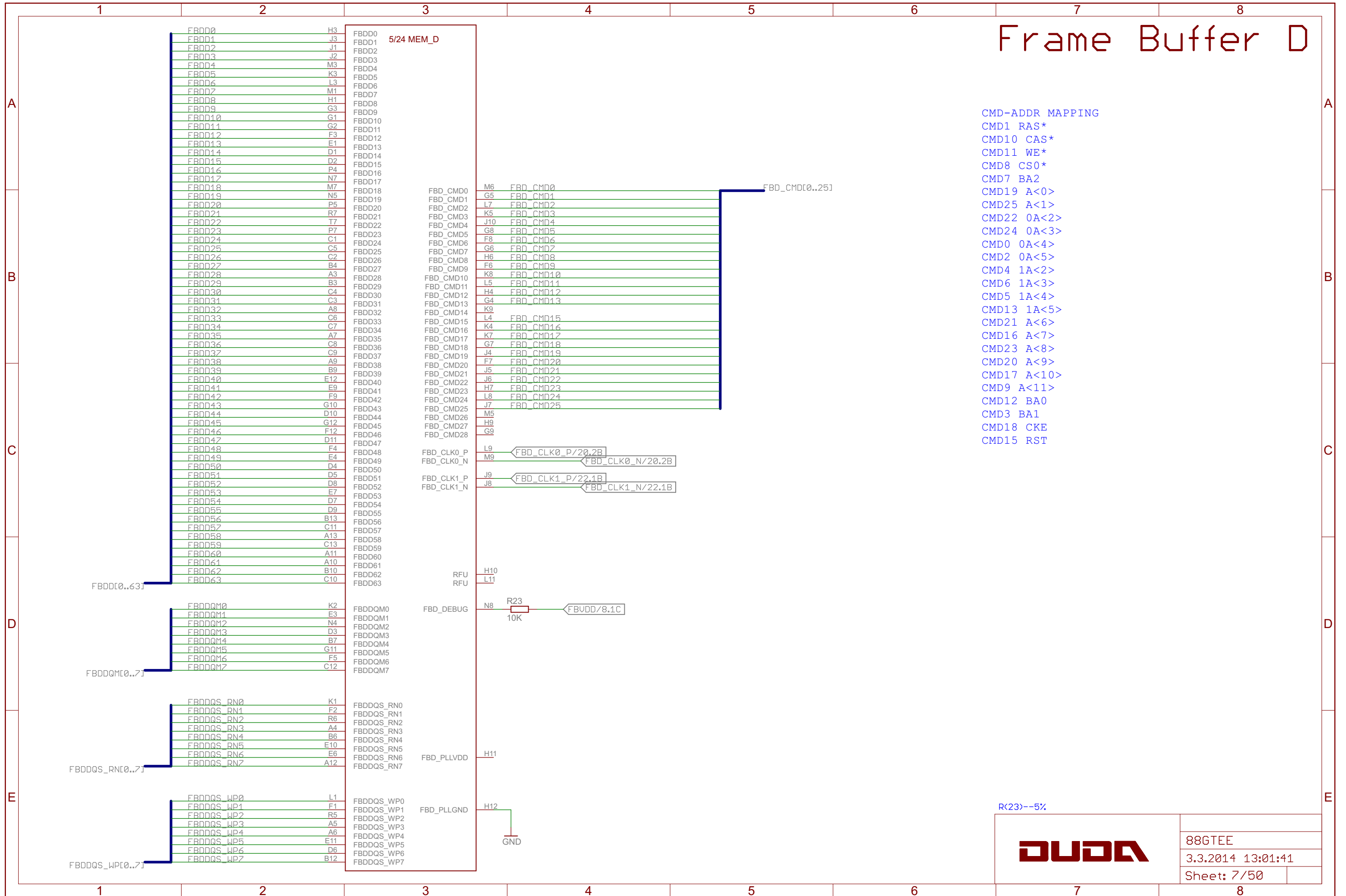




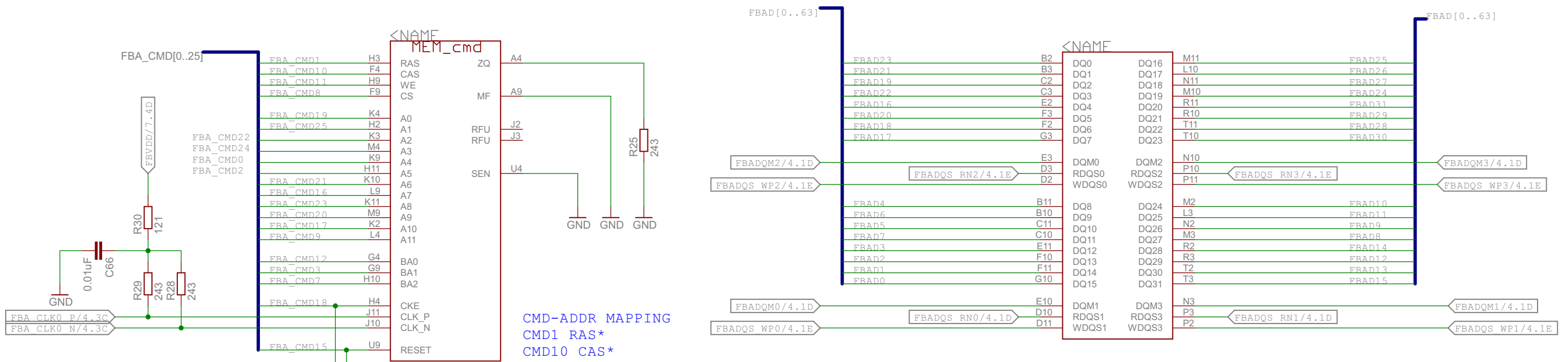
# Frame Buffer D

## CMD-ADDR MAPPING

- CMD1 RAS\*
- CMD10 CAS\*
- CMD11 WE\*
- CMD8 CS0\*
- CMD7 BA2
- CMD19 A<0>
- CMD25 A<1>
- CMD22 0A<2>
- CMD24 0A<3>
- CMD0 0A<4>
- CMD2 0A<5>
- CMD4 1A<2>
- CMD6 1A<3>
- CMD5 1A<4>
- CMD13 1A<5>
- CMD21 A<6>
- CMD16 A<7>
- CMD23 A<8>
- CMD20 A<9>
- CMD17 A<10>
- CMD9 A<11>
- CMD12 BA0
- CMD3 BA1
- CMD18 CKE
- CMD15 RST



# FBA-LOW32B



### CMD-ADDR MAPPING

- CMD1 RAS\*
- CMD10 CAS\*
- CMD11 WE\*
- CMD8 CS0\*
- CMD7 BA2
- CMD19 A<0>
- CMD25 A<1>
- CMD22 0A<2>
- CMD24 0A<3>
- CMD0 0A<4>
- CMD2 0A<5>
- CMD4 1A<2>
- CMD6 1A<3>
- CMD5 1A<4>
- CMD13 1A<5>
- CMD21 A<6>
- CMD16 A<7>
- CMD23 A<8>
- CMD20 A<9>
- CMD17 A<10>
- CMD9 A<11>
- CMD12 BA0
- CMD3 BA1
- CMD18 CKE
- CMD15 RST

### MEM PIN SWITCH MIRROR

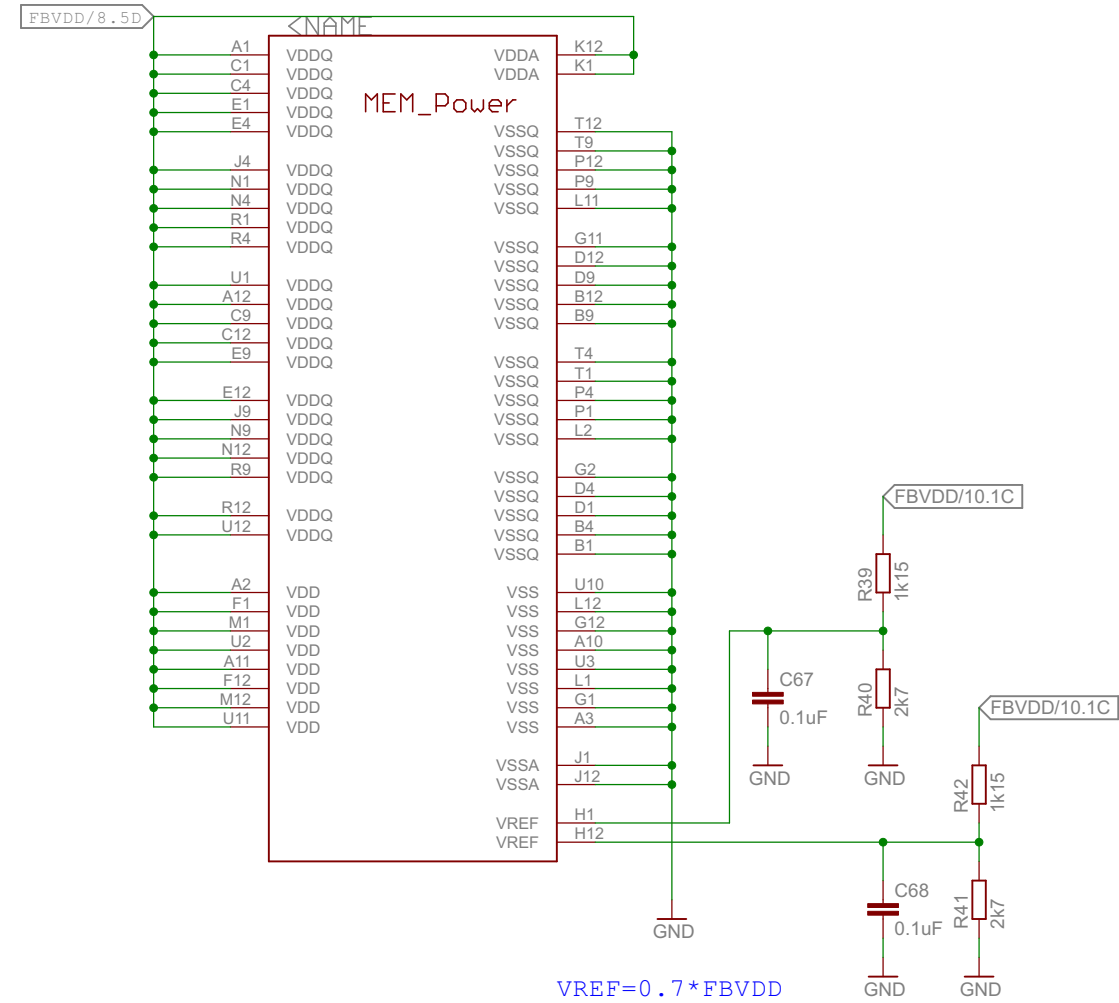
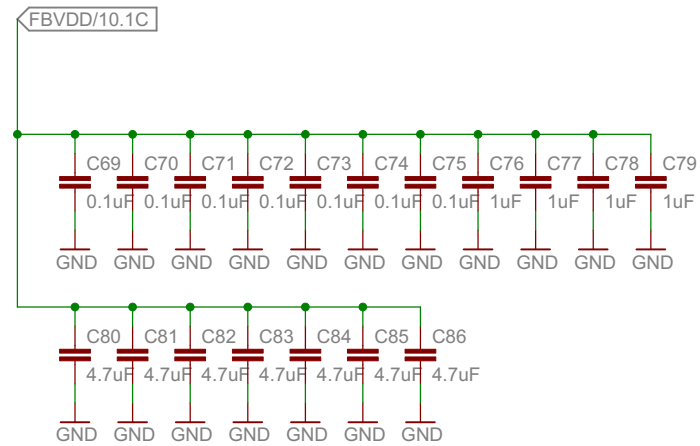
- MF LOGIC STATE  
HIGH LOW
- RAS# H10 H3
  - CAS# F9 F4
  - WE# H4 H9
  - CS# F4 F9
  - CKE H9 H4
  - A0 K9 K4
  - A1 H11 H2
  - A2 K10 K3
  - A3 M9 M4
  - A4 K4 K9
  - A5 H2 H11
  - A6 K3 K10
  - A7 L4 L9
  - A8 K2 K11
  - A9 M4 M9
  - A10 K11 K2
  - BA0 G9 G4
  - BA1 G4 G9
  - BA2 H3 H10

R(25-27)--1%  
R(28-38)--5%  
C(66)--X7R/16V/10%





# FBA-LOW32B-Power



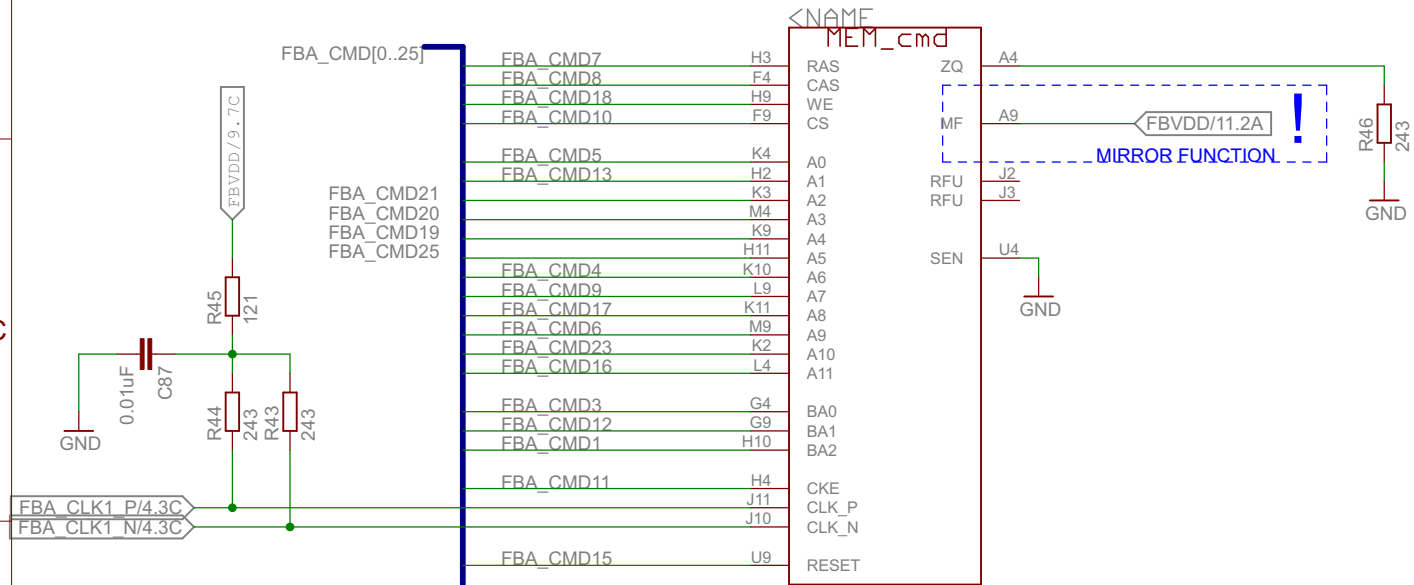
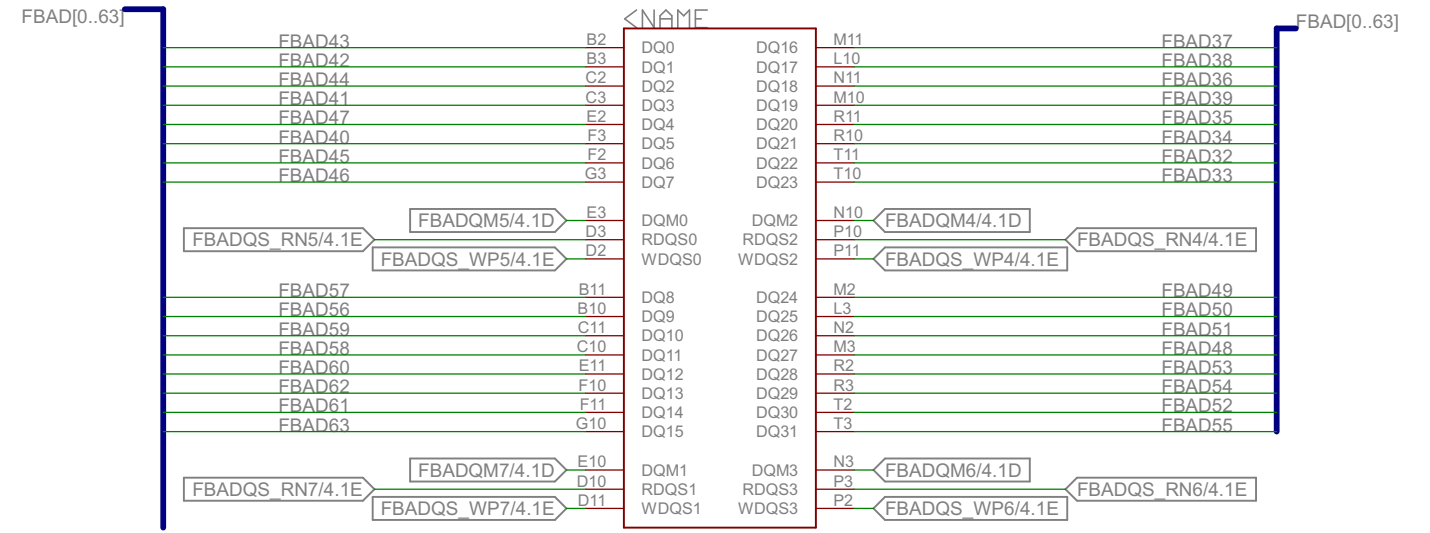
R(39-42)--1%

C(67-75)--X5R/10V/10%  
C(76-85)--X5R/6.3V/10%

**DUDA**

88GTEE  
3.3.2014 13:01:41  
Sheet: 9/50

# FBA-HIGH32B



## CMD-ADDR MAPPING

CMD1 RAS\*  
 CMD10 CAS\*  
 CMD11 WE\*  
 CMD8 CS0\*  
 CMD7 BA2  
 CMD19 A<0>  
 CMD25 A<1>  
 CMD22 0A<2>  
 CMD24 0A<3>  
 CMD0 0A<4>  
 CMD2 0A<5>  
 CMD4 1A<2>  
 CMD6 1A<3>  
 CMD5 1A<4>  
 CMD13 1A<5>  
 CMD21 A<6>  
 CMD16 A<7>  
 CMD23 A<8>  
 CMD20 A<9>  
 CMD17 A<10>  
 CMD9 A<11>  
 CMD12 BA0  
 CMD3 BA1  
 CMD18 CKE  
 CMD15 RST

## MEM PIN SWITCH MIRROR

MF LOGIC STATE  
 HIGH LOW  
 RAS# H10 H3  
 CAS# F9 F4  
 WE# H4 H9  
 CS# F4 F9  
 CKE H9 H4  
 A0 K9 K4  
 A1 H11 H2  
 A2 K10 K3  
 A3 M9 M4  
 A4 K4 K9  
 A5 H2 H11  
 A6 K3 K10  
 A7 L4 L9  
 A8 K2 K11  
 A9 M4 M9  
 A10 K11 K2  
 A11 L9 L4  
 BA0 G9 G4  
 BA1 G4 G9  
 BA2 H3 H10

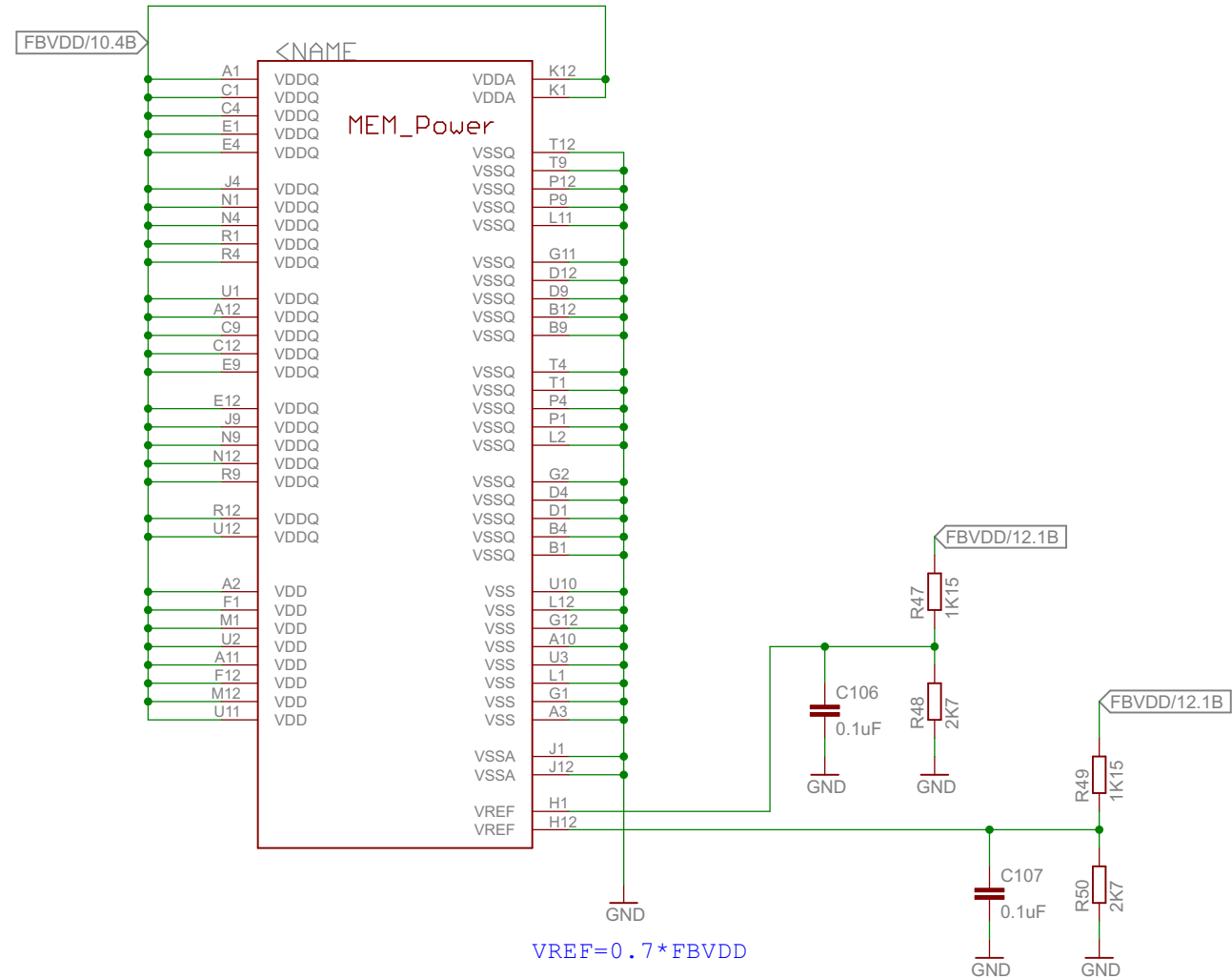
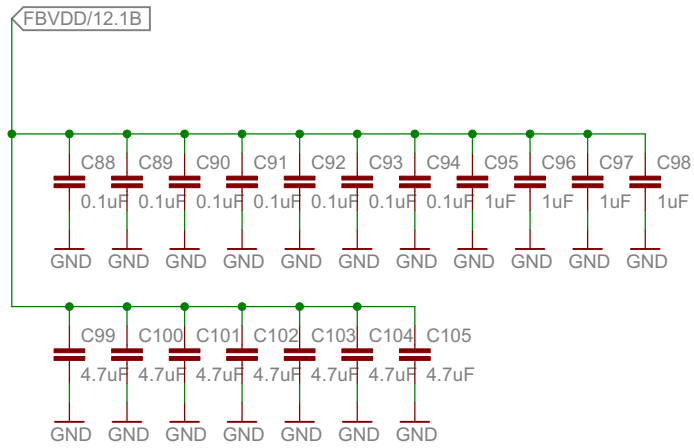
R(46)--1%  
R(43-45)--5%

C(87)--X7R/16V/10%



88GTEE  
 3.3.2014 13:01:41  
 Sheet: 10/50

# FBA-HIGH32B-Power



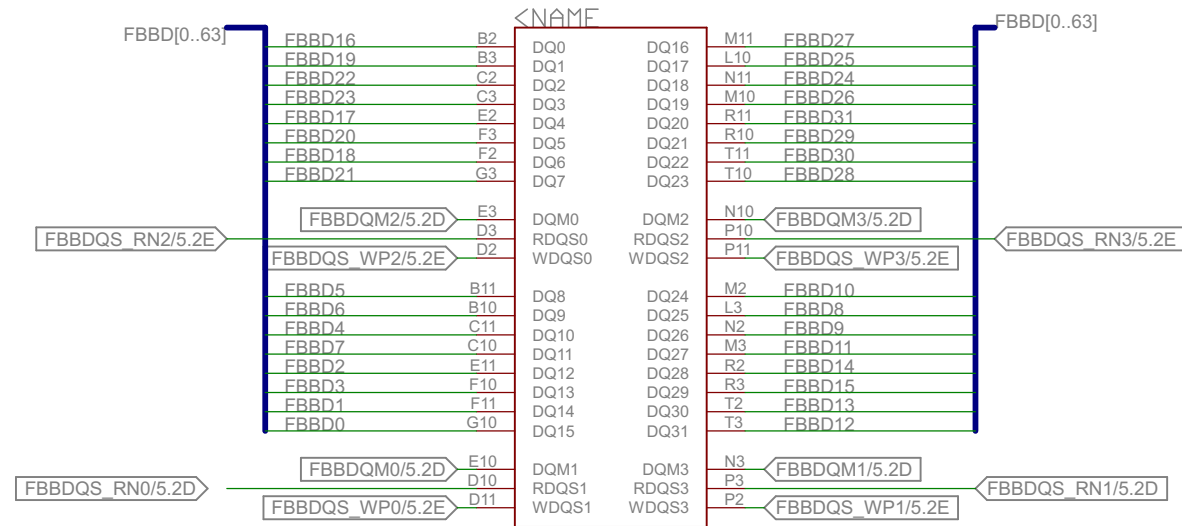
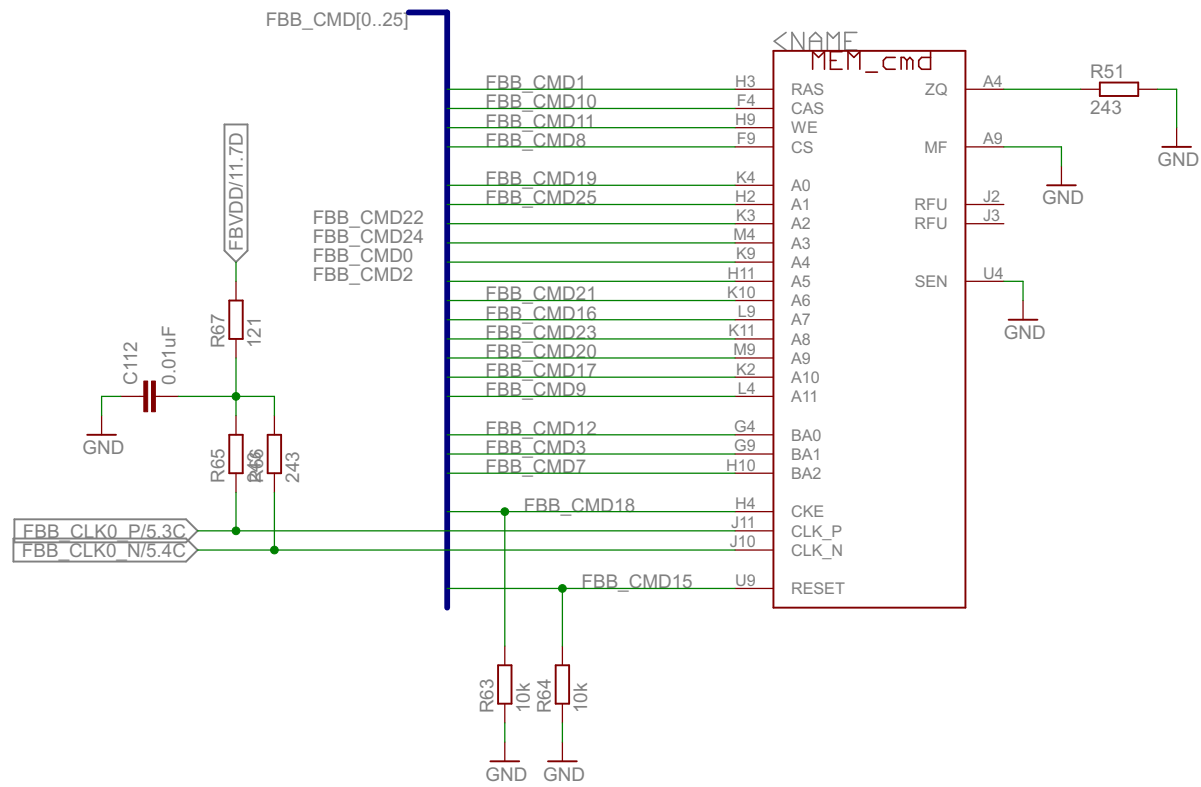
R(47-50)--1%

C(88-94,106-107)--X5R/10V/10%  
C(95-105)--X5R/6.3V/10%



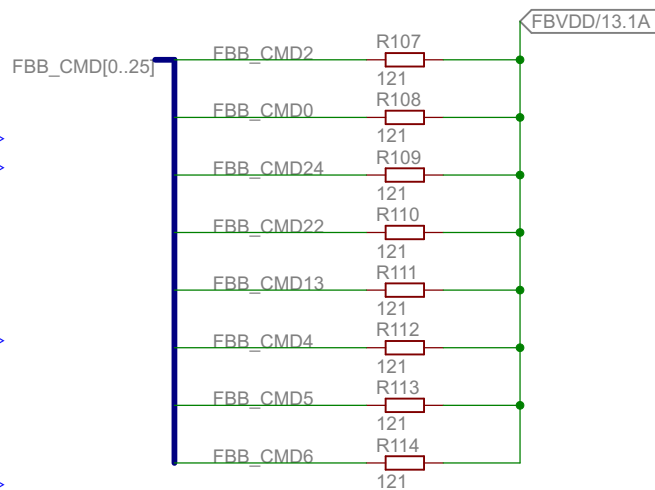
88GTEE  
3.3.2014 13:01:41  
Sheet: 11/50

# FBB-LOW32B



## CMD-ADDR MAPPING

CMD1 RAS\*  
 CMD10 CAS\*  
 CMD11 WE\*  
 CMD8 CS0\*  
 CMD7 BA2  
 CMD19 A<0>  
 CMD25 A<1>  
 CMD22 0A<2>  
 CMD24 0A<3>  
 CMD0 0A<4>  
 CMD2 0A<5>  
 CMD4 1A<2>  
 CMD6 1A<3>  
 CMD5 1A<4>  
 CMD13 1A<5>  
 CMD21 A<6>  
 CMD16 A<7>  
 CMD23 A<8>  
 CMD20 A<9>  
 CMD17 A<10>  
 CMD9 A<11>  
 CMD12 BA0  
 CMD3 BA1  
 CMD18 CKE  
 CMD15 RST



## MEM PIN SWITCH MIRROR

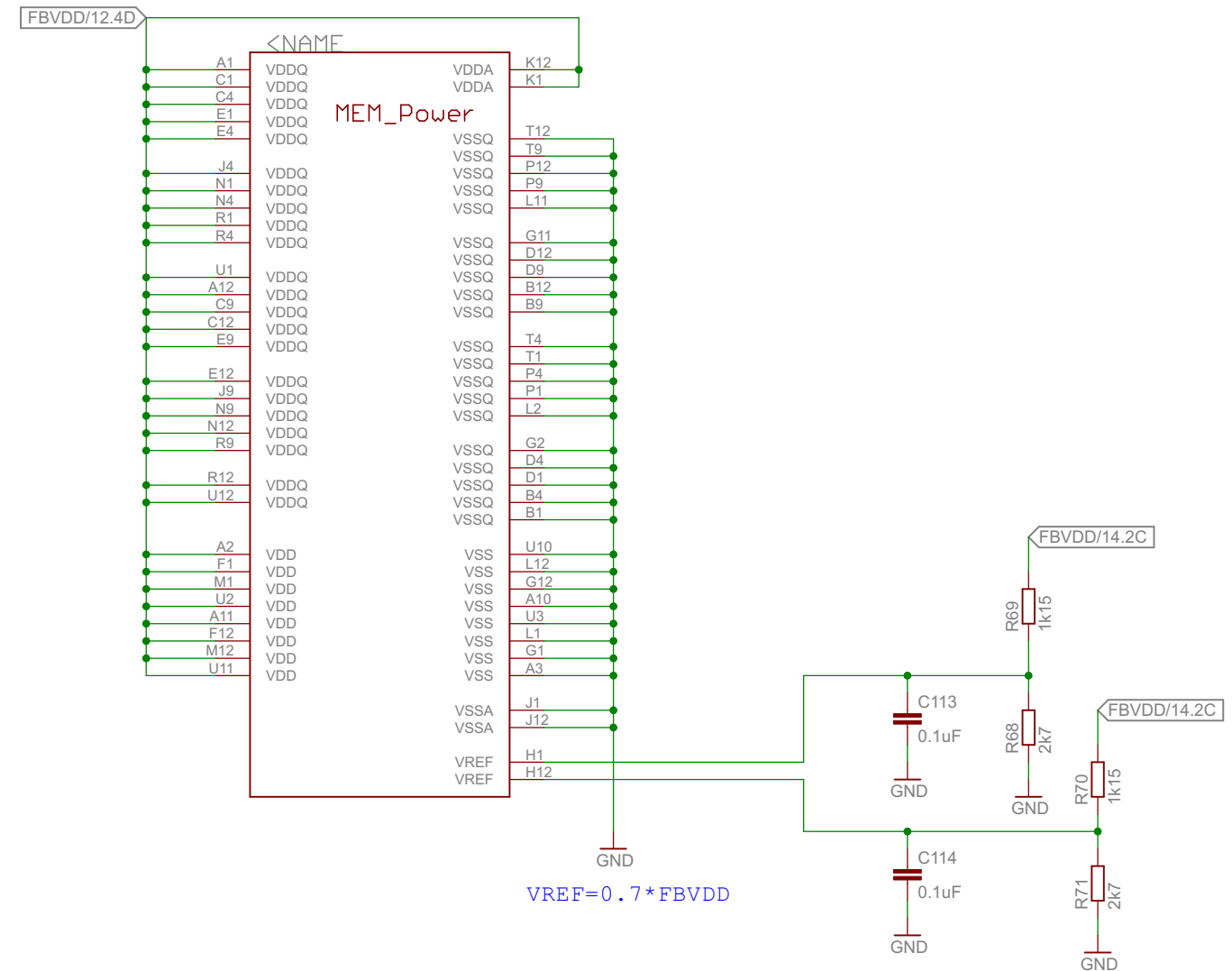
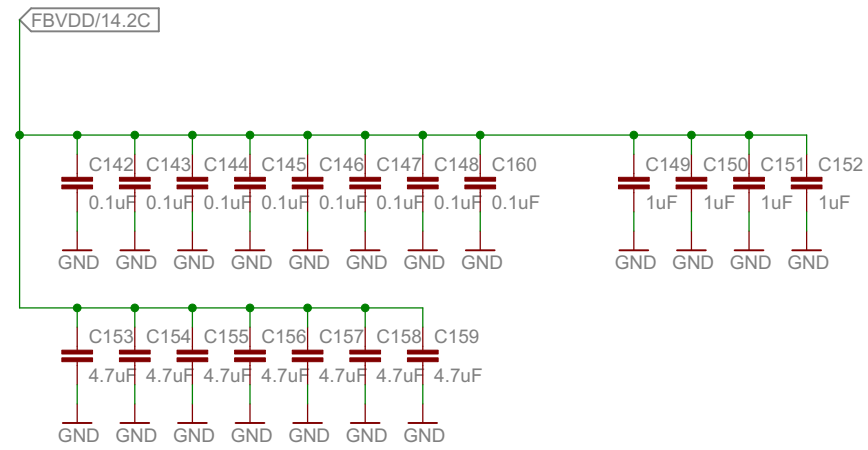
MF LOGIC STATE  
 HIGH LOW  
 RAS# H10 H3  
 CAS# F9 F4  
 WE# H4 H9  
 CS# F4 F9  
 CKE H9 H4  
 A0 K9 K4  
 A1 H11 H2  
 A2 K10 K3  
 A3 M9 M4  
 A4 K4 K9  
 A5 H2 H11  
 A6 K3 K10  
 A7 L4 L9  
 A8 K2 K11  
 A9 M4 M9  
 A10 K11 K2  
 A11 L9 L4  
 BA0 G9 G4  
 BA1 G4 G9  
 BA2 H3 H10

R(51,63-64)--1%  
 R(65-67)--5%  
 C(112)--X7R/16V/10%



88GTEE  
 3.3.2014 13:01:41  
 Sheet: 12/50

# FBB-LOW32B-Power

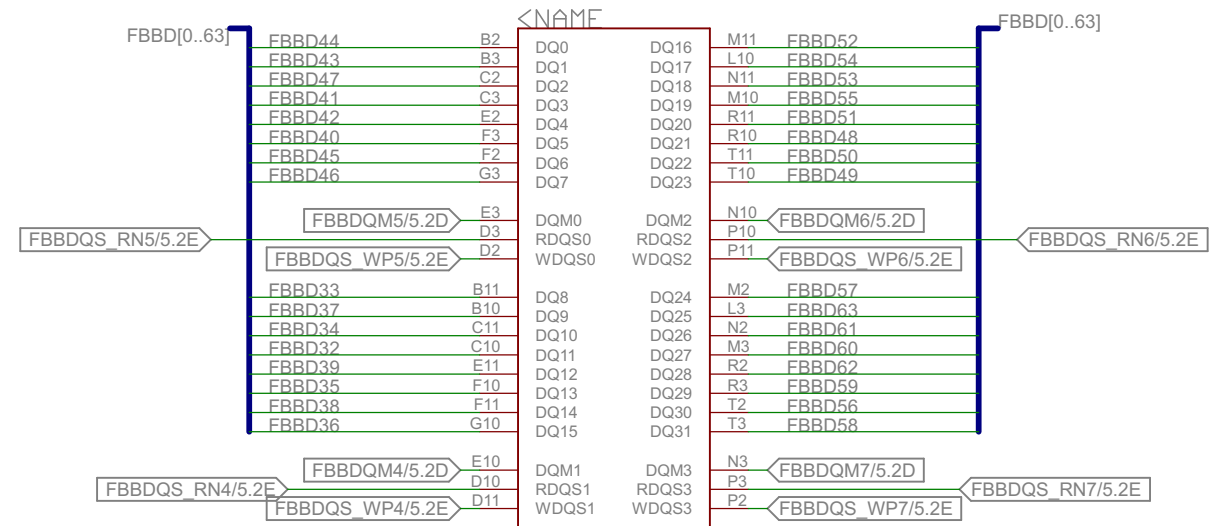
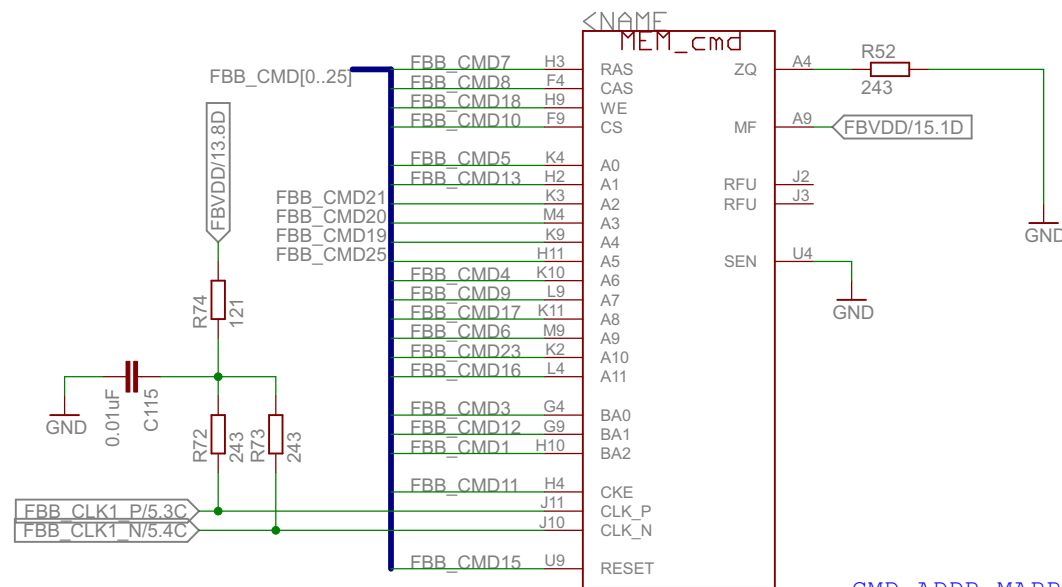


R(68-71)--1%  
RC(113-114)--X5R/10V/10%



88GTEE  
3.3.2014 13:01:41  
Sheet: 13/50

# FBB-HIGH32B



## CMD-ADDR MAPPING

```

CMD1 RAS*
CMD10 CAS*
CMD11 WE*
CMD8 CS0*
CMD7 BA2
CMD19 A<0>
CMD25 A<1>
CMD22 0A<2>
CMD24 0A<3>
CMD0 0A<4>
CMD2 0A<5>
CMD4 1A<2>
CMD6 1A<3>
CMD5 1A<4>
CMD13 1A<5>
CMD21 A<6>
CMD16 A<7>
CMD23 A<8>
CMD20 A<9>
CMD17 A<10>
CMD9 A<11>
CMD12 BA0
CMD3 BA1
CMD18 CKE
CMD15 RST
    
```

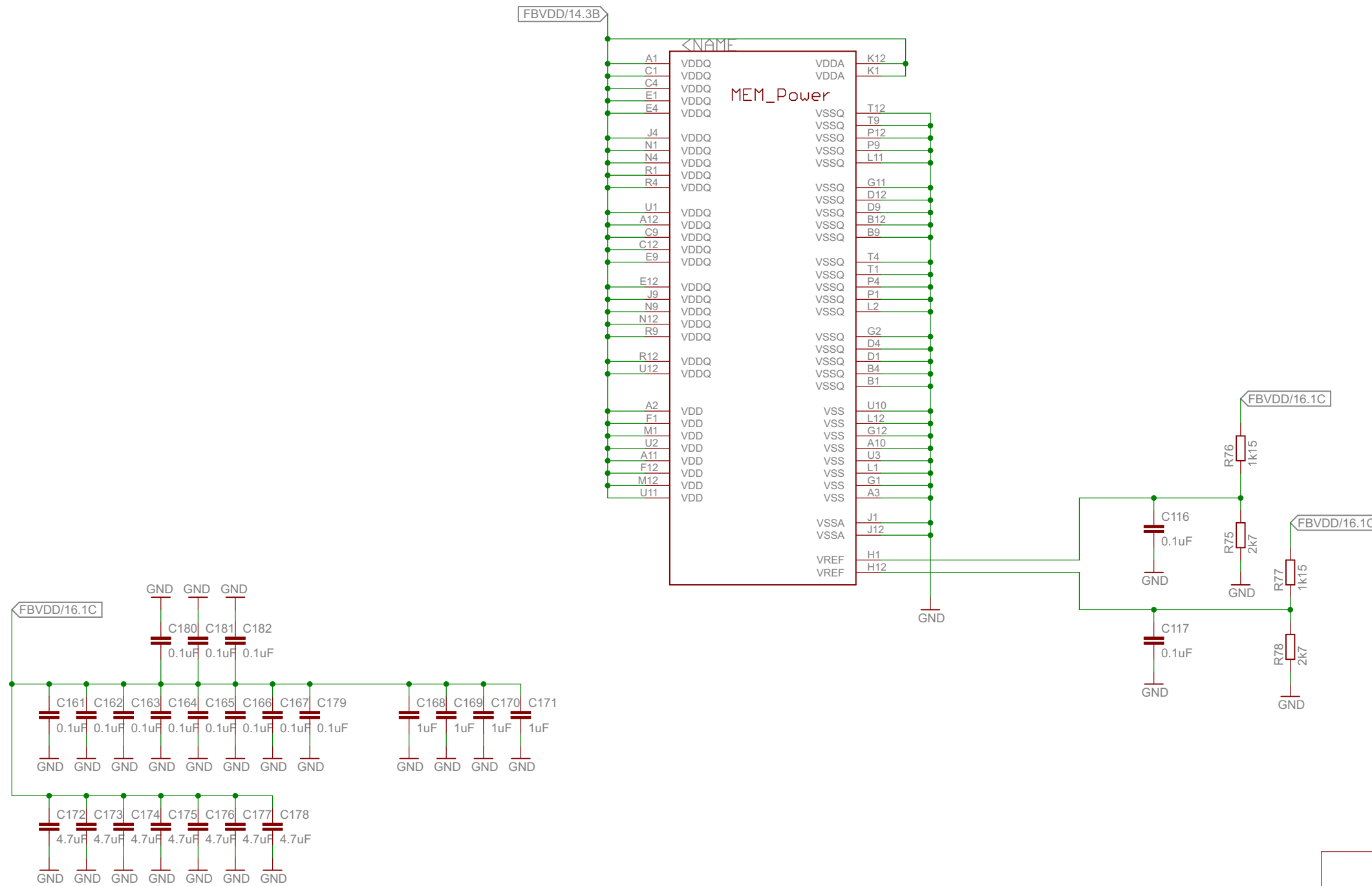
## MEM PIN SWITCH MIRROR

```

MF LOGIC STATE
HIGH LOW
RAS# H10 H3
CAS# F9 F4
WE# H4 H9
CS# F4 F9
CKE H9 H4
A0 K9 K4
A1 H11 H2
A2 K10 K3
A3 M9 M4
A4 K4 K9
A5 H2 H11
A6 K3 K10
A7 L4 L9
A8 K2 K11
A9 M4 M9
A10 K11 K2
A11 L9 L4
BA0 G9 G4
BA1 G4 G9
BA2 H3 H10
    
```



# FBB-HIGH32B-Power



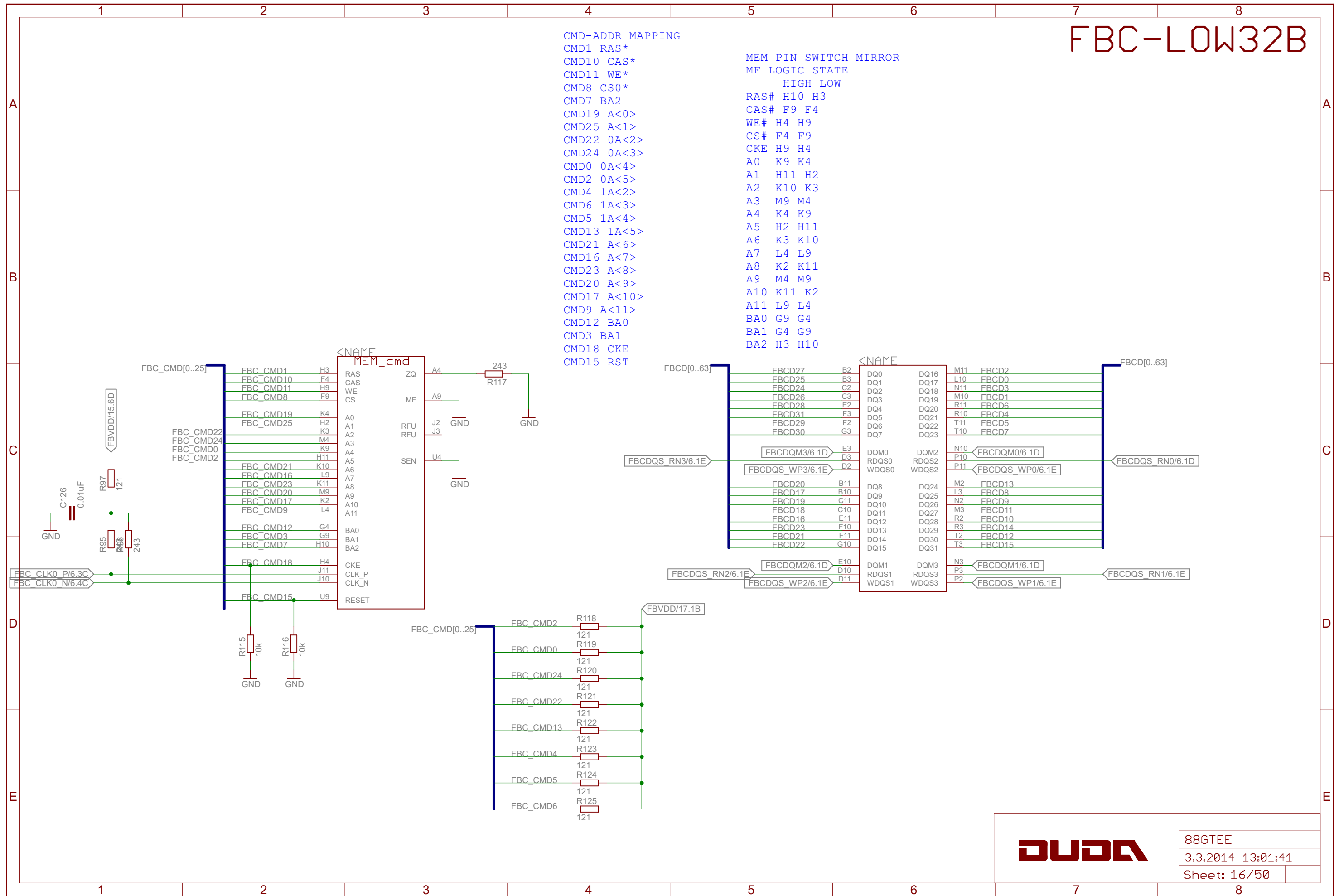
88GTEE  
 3.3.2014 13:01:41  
 Sheet: 15/50



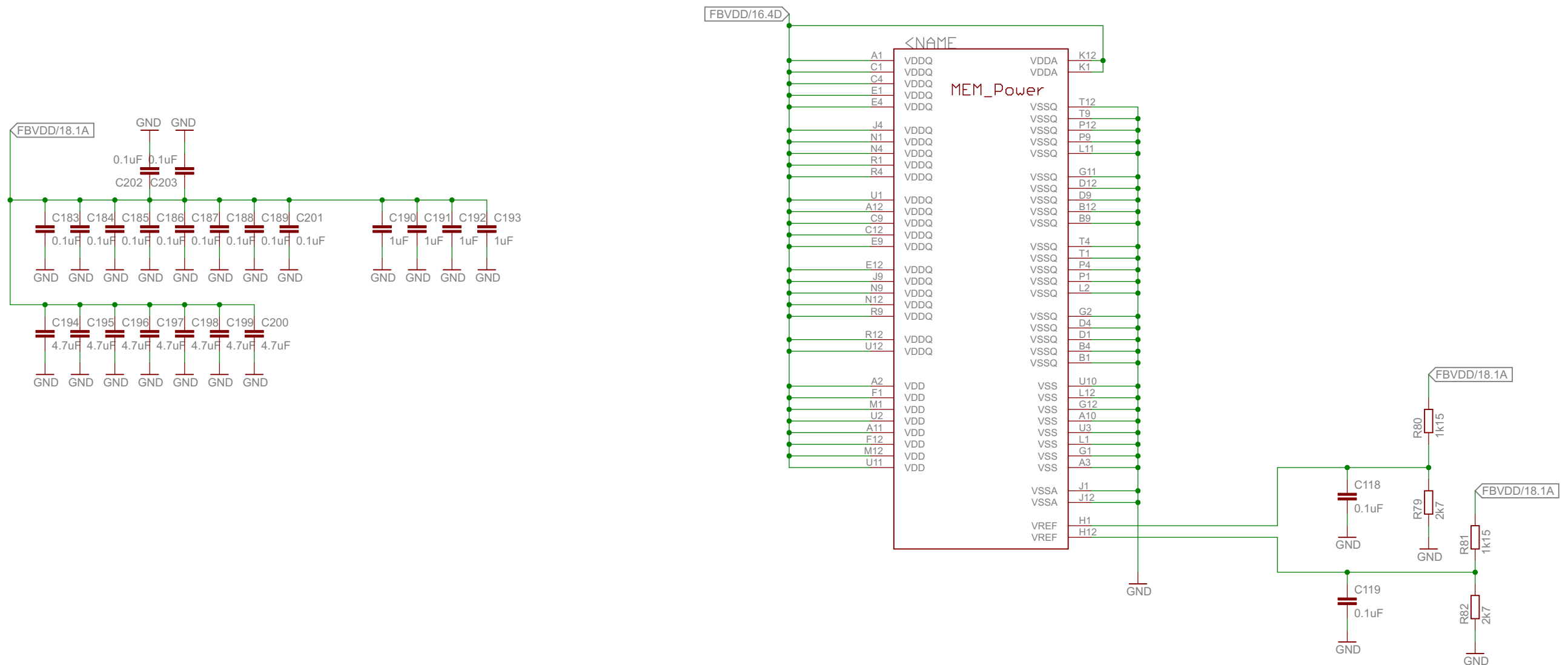
# FBC-LOW32B

## CMD-ADDR MAPPING

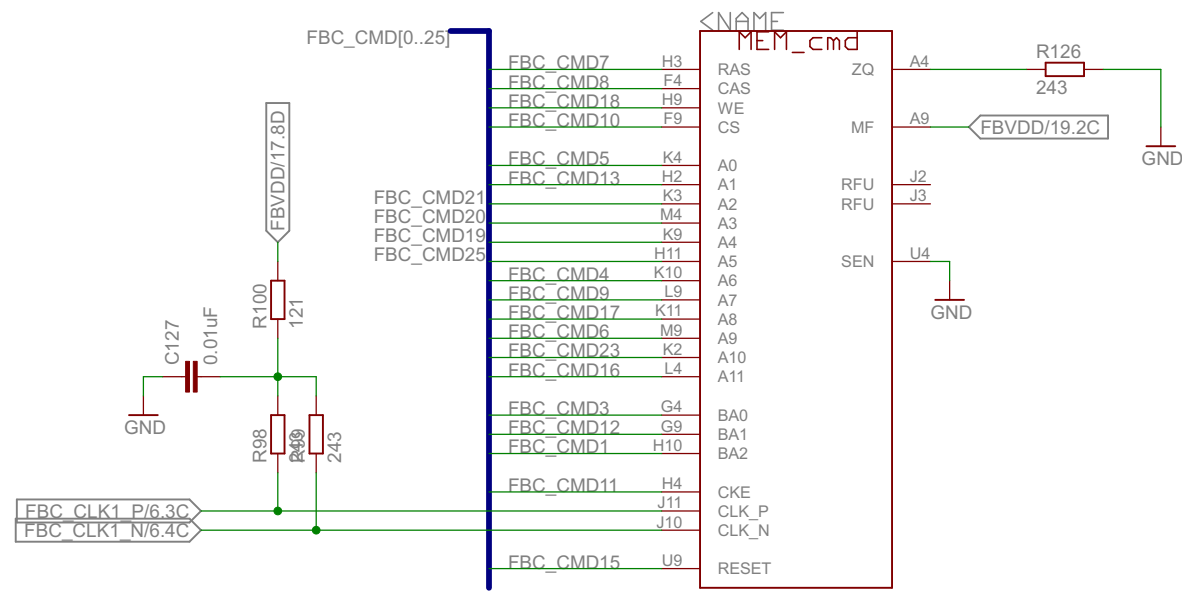
CMD1 RAS*	MEM PIN SWITCH MIRROR
CMD10 CAS*	MF LOGIC STATE
CMD11 WE*	HIGH LOW
CMD8 CS0*	RAS# H10 H3
CMD7 BA2	CAS# F9 F4
CMD19 A<0>	WE# H4 H9
CMD25 A<1>	CS# F4 F9
CMD22 0A<2>	CKE H9 H4
CMD24 0A<3>	A0 K9 K4
CMD0 0A<4>	A1 H11 H2
CMD2 0A<5>	A2 K10 K3
CMD4 1A<2>	A3 M9 M4
CMD6 1A<3>	A4 K4 K9
CMD5 1A<4>	A5 H2 H11
CMD13 1A<5>	A6 K3 K10
CMD21 A<6>	A7 L4 L9
CMD16 A<7>	A8 K2 K11
CMD23 A<8>	A9 M4 M9
CMD20 A<9>	A10 K11 K2
CMD17 A<10>	A11 L9 L4
CMD9 A<11>	BA0 G9 G4
CMD12 BA0	BA1 G4 G9
CMD3 BA1	BA2 H3 H10
CMD18 CKE	
CMD15 RST	



# FBC-LOW32B-Power



# FBC-HIGH32B

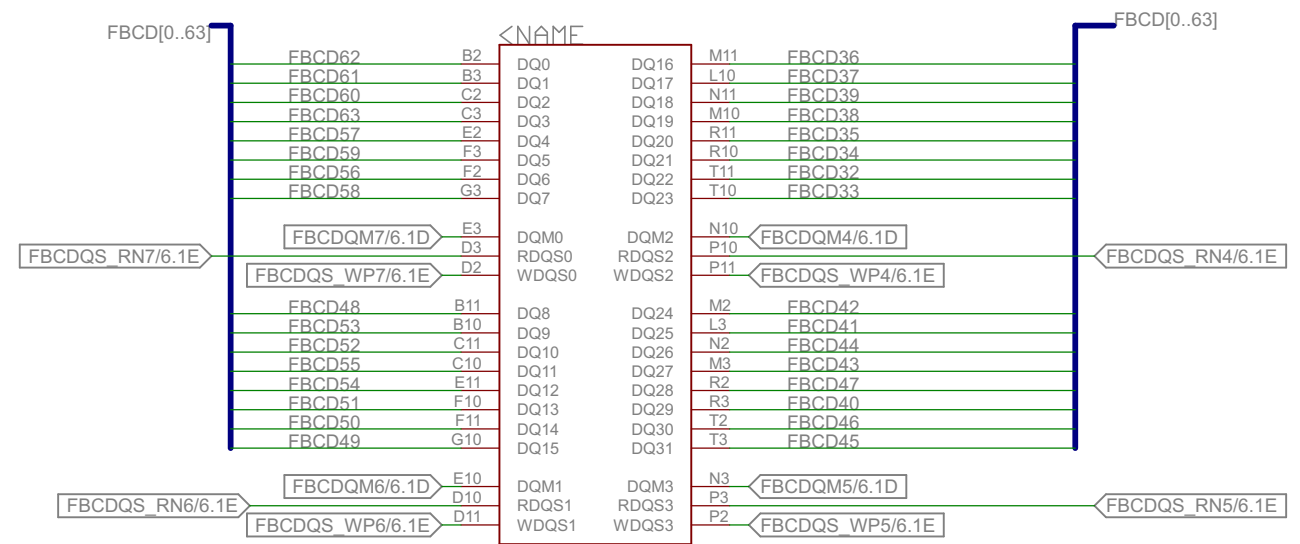


## CMD-ADDR MAPPING

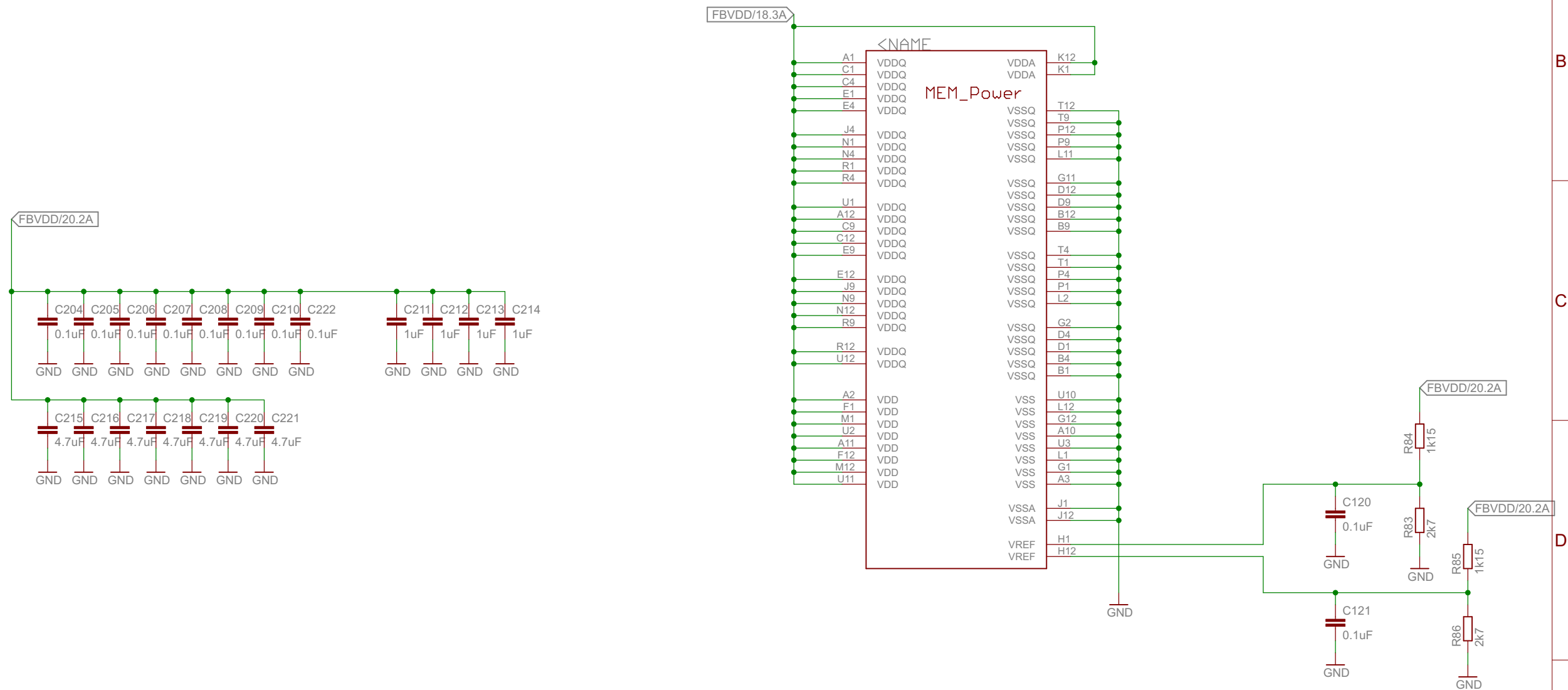
CMD1 RAS*	
CMD10 CAS*	
CMD11 WE*	
CMD8 CS0*	
CMD7 BA2	
CMD19 A<0>	
CMD25 A<1>	
CMD22 0A<2>	
CMD24 0A<3>	
CMD0 0A<4>	
CMD2 0A<5>	
CMD4 1A<2>	
CMD6 1A<3>	
CMD5 1A<4>	
CMD13 1A<5>	
CMD21 A<6>	
CMD16 A<7>	
CMD23 A<8>	
CMD20 A<9>	
CMD17 A<10>	
CMD9 A<11>	
CMD12 BA0	
CMD3 BA1	
CMD18 CKE	
CMD15 RST	

	MEM PIN SWITCH MIRROR
	MF LOGIC STATE
	HIGH LOW
RAS# H10 H3	
CAS# F9 F4	
WE# H4 H9	
CS# F4 F9	
CKE H9 H4	
A0 K9 K4	
A1 H11 H2	
A2 K10 K3	
A3 M9 M4	
A4 K4 K9	
A5 H2 H11	
A6 K3 K10	
A7 L4 L9	
A8 K2 K11	
A9 M4 M9	
A10 K11 K2	
A11 L9 L4	
BA0 G9 G4	
BA1 G4 G9	
BA2 H3 H10	

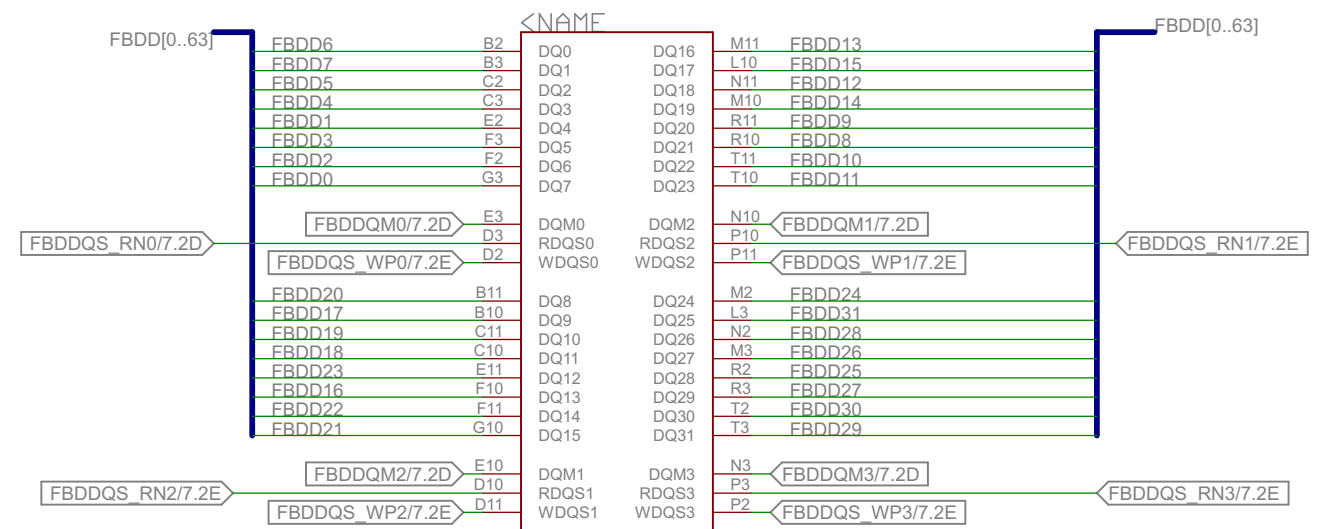
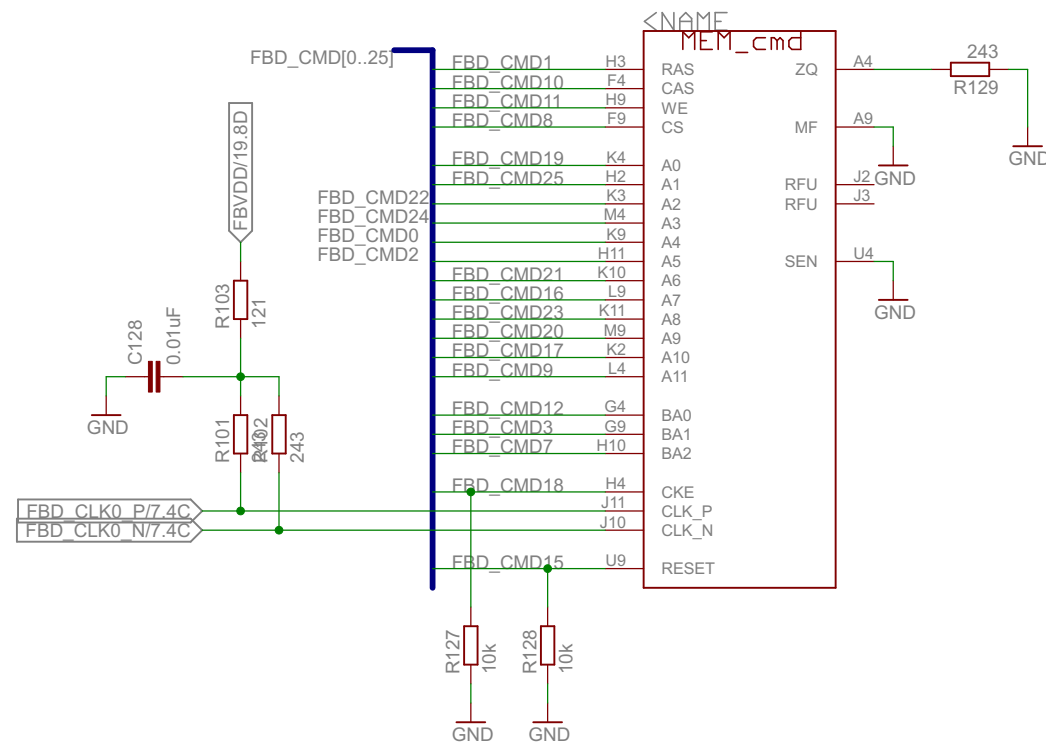


# FBC-HIGH32B-Power



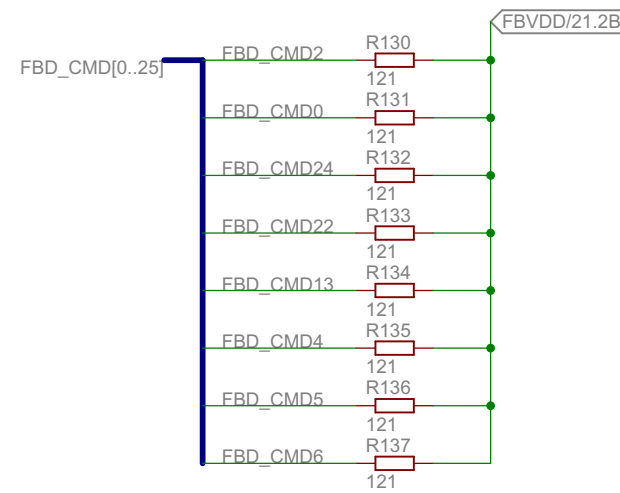
88GTEE  
 3.3.2014 13:01:41  
 Sheet: 19/50

# FBD-LOW32B

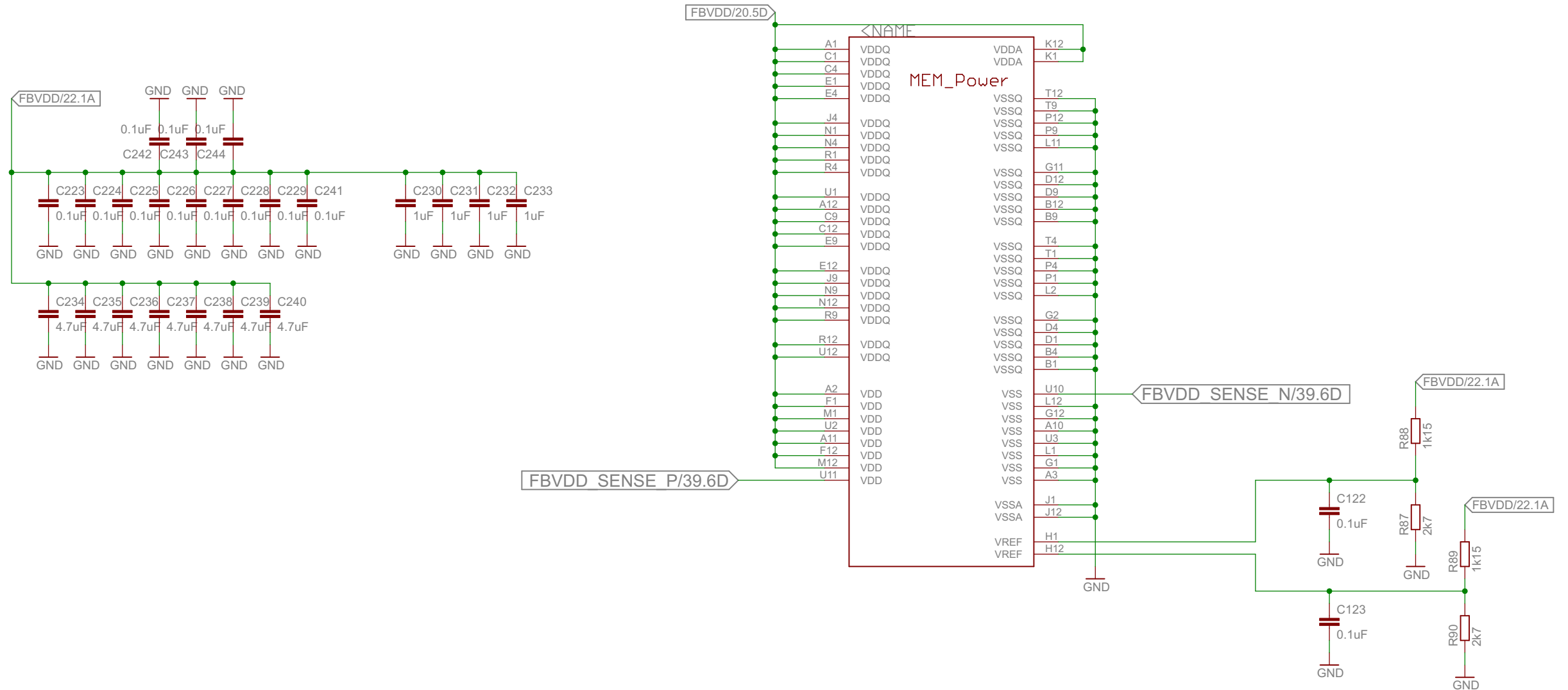


## CMD-ADDR MAPPING

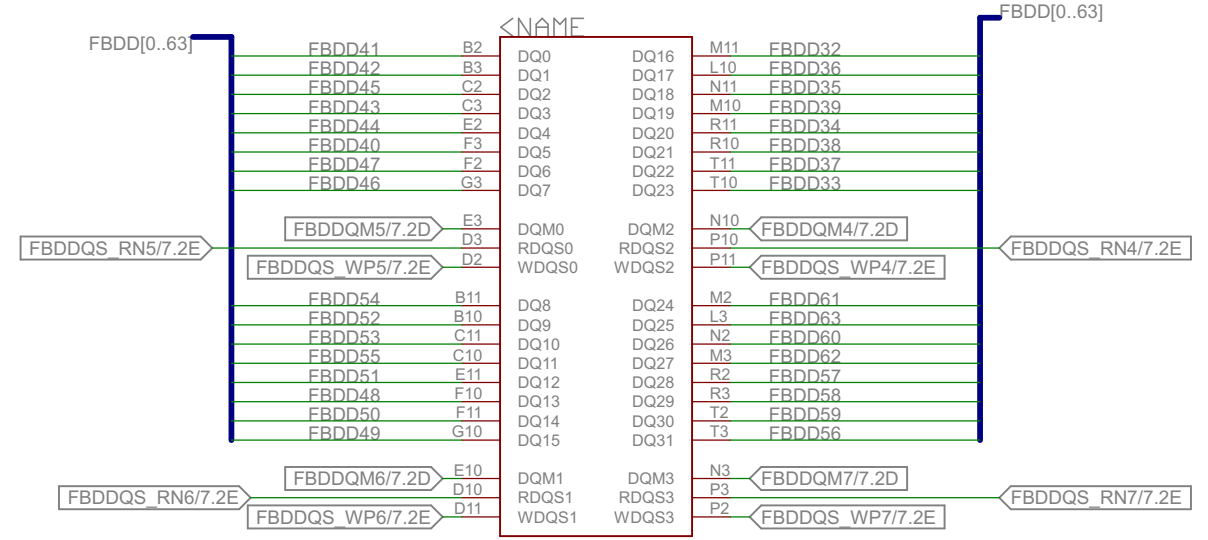
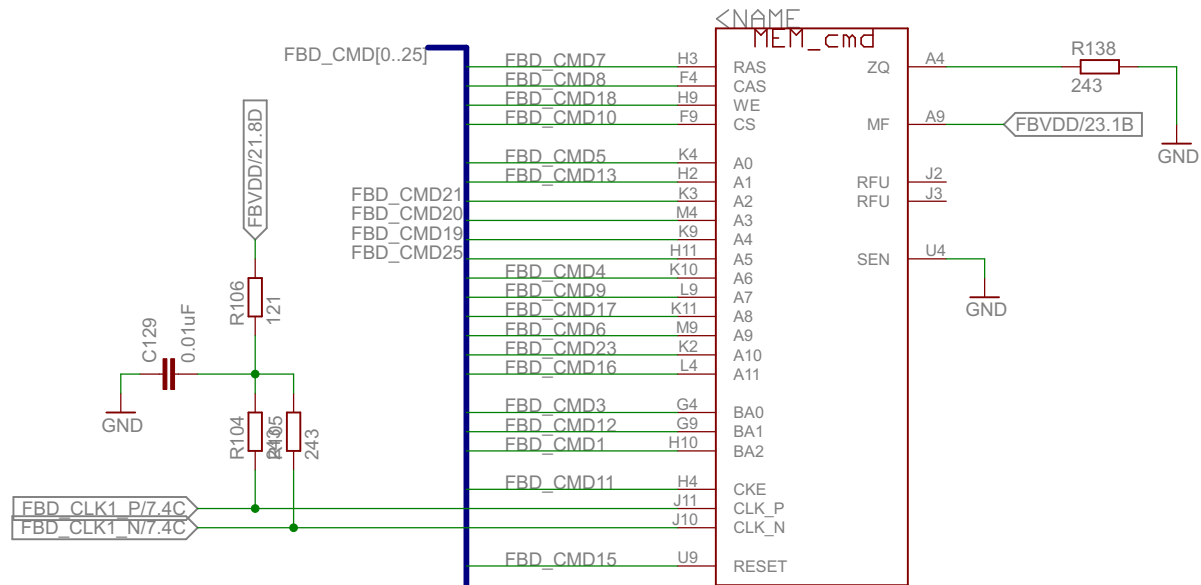
CMD1 RAS*	MEM PIN SWITCH MIRROR
CMD10 CAS*	MF LOGIC STATE
CMD11 WE*	HIGH LOW
CMD8 CS0*	RAS# H10 H3
CMD7 BA2	CAS# F9 F4
CMD19 A<0>	WE# H4 H9
CMD25 A<1>	CS# F4 F9
CMD22 0A<2>	CKE H9 H4
CMD24 0A<3>	A0 K9 K4
CMD0 0A<4>	A1 H11 H2
CMD2 0A<5>	A2 K10 K3
CMD4 1A<2>	A3 M9 M4
CMD6 1A<3>	A4 K4 K9
CMD5 1A<4>	A5 H2 H11
CMD13 1A<5>	A6 K3 K10
CMD21 A<6>	A7 L4 L9
CMD16 A<7>	A8 K2 K11
CMD23 A<8>	A9 M4 M9
CMD20 A<9>	A10 K11 K2
CMD17 A<10>	A11 L9 L4
CMD9 A<11>	BA0 G9 G4
CMD12 BA0	BA1 G4 G9
CMD3 BA1	BA2 H3 H10
CMD18 CKE	
CMD15 RST	



# FBD-LOW32B-Power



# FBD-HIGH32B



### CMD-ADDR MAPPING

CMD1 RAS\*  
 CMD10 CAS\*  
 CMD11 WE\*  
 CMD8 CS0\*  
 CMD7 BA2  
 CMD19 A<0>  
 CMD25 A<1>  
 CMD22 0A<2>  
 CMD24 0A<3>  
 CMD0 0A<4>  
 CMD2 0A<5>  
 CMD4 1A<2>  
 CMD6 1A<3>  
 CMD5 1A<4>  
 CMD13 1A<5>  
 CMD21 A<6>  
 CMD16 A<7>  
 CMD23 A<8>  
 CMD20 A<9>  
 CMD17 A<10>  
 CMD9 A<11>  
 CMD12 BA0  
 CMD3 BA1  
 CMD18 CKE  
 CMD15 RST

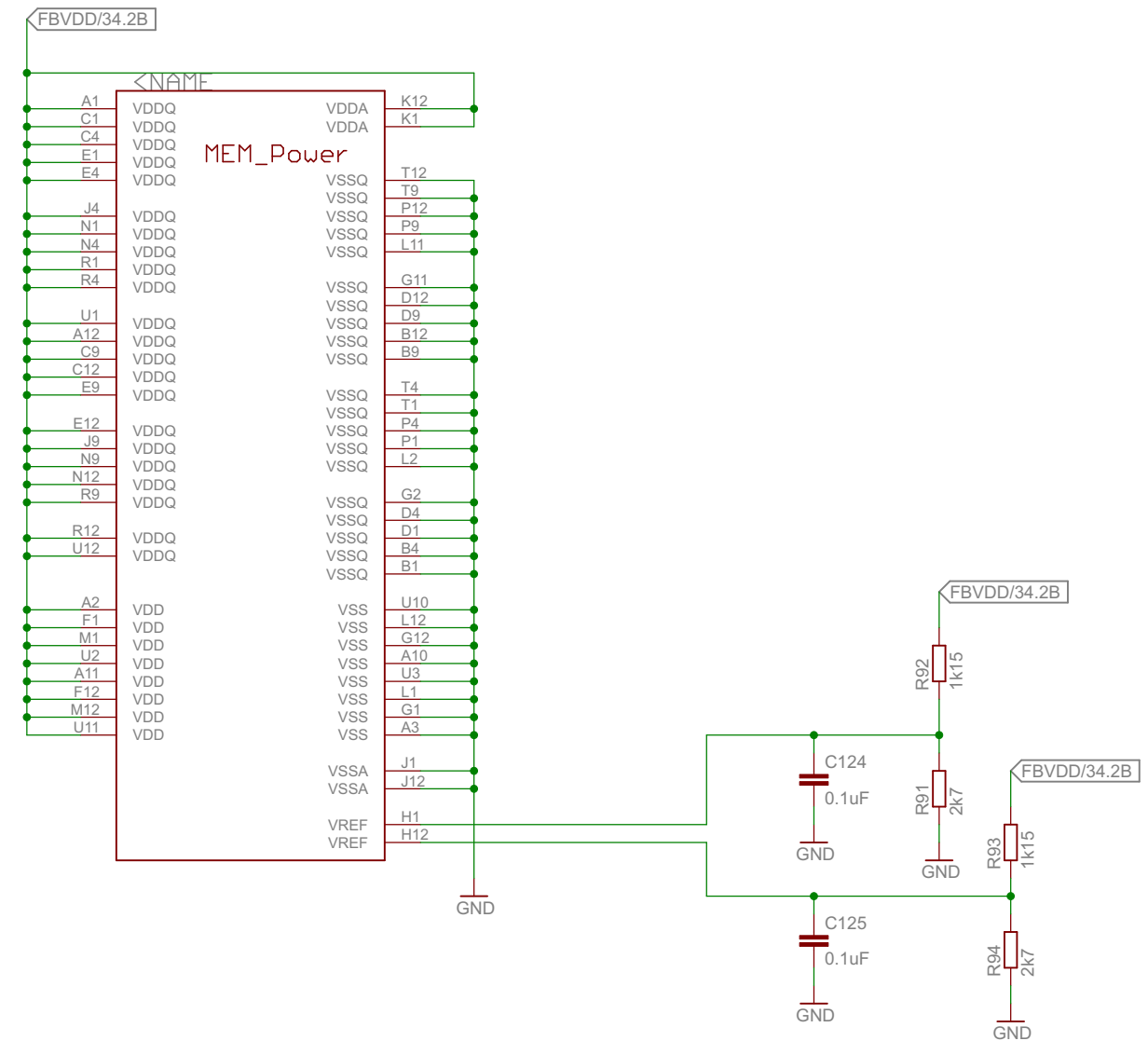
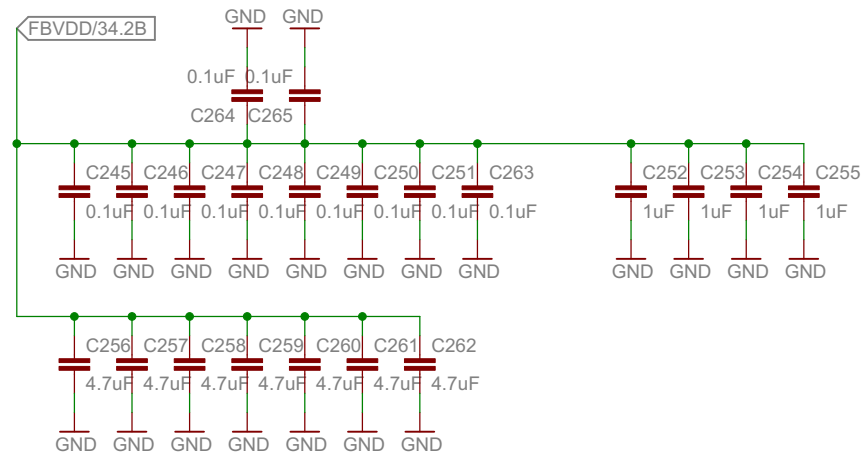
### MEM PIN SWITCH MIRROR

MF LOGIC STATE  
 HIGH LOW  
 RAS# H10 H3  
 CAS# F9 F4  
 WE# H4 H9  
 CS# F4 F9  
 CKE H9 H4  
 A0 K9 K4  
 A1 H11 H2  
 A2 K10 K3  
 A3 M9 M4  
 A4 K4 K9  
 A5 H2 H11  
 A6 K3 K10  
 A7 L4 L9  
 A8 K2 K11  
 A9 M4 M9  
 A10 K11 K2  
 A11 L9 L4  
 BA0 G9 G4  
 BA1 G4 G9  
 BA2 H3 H10





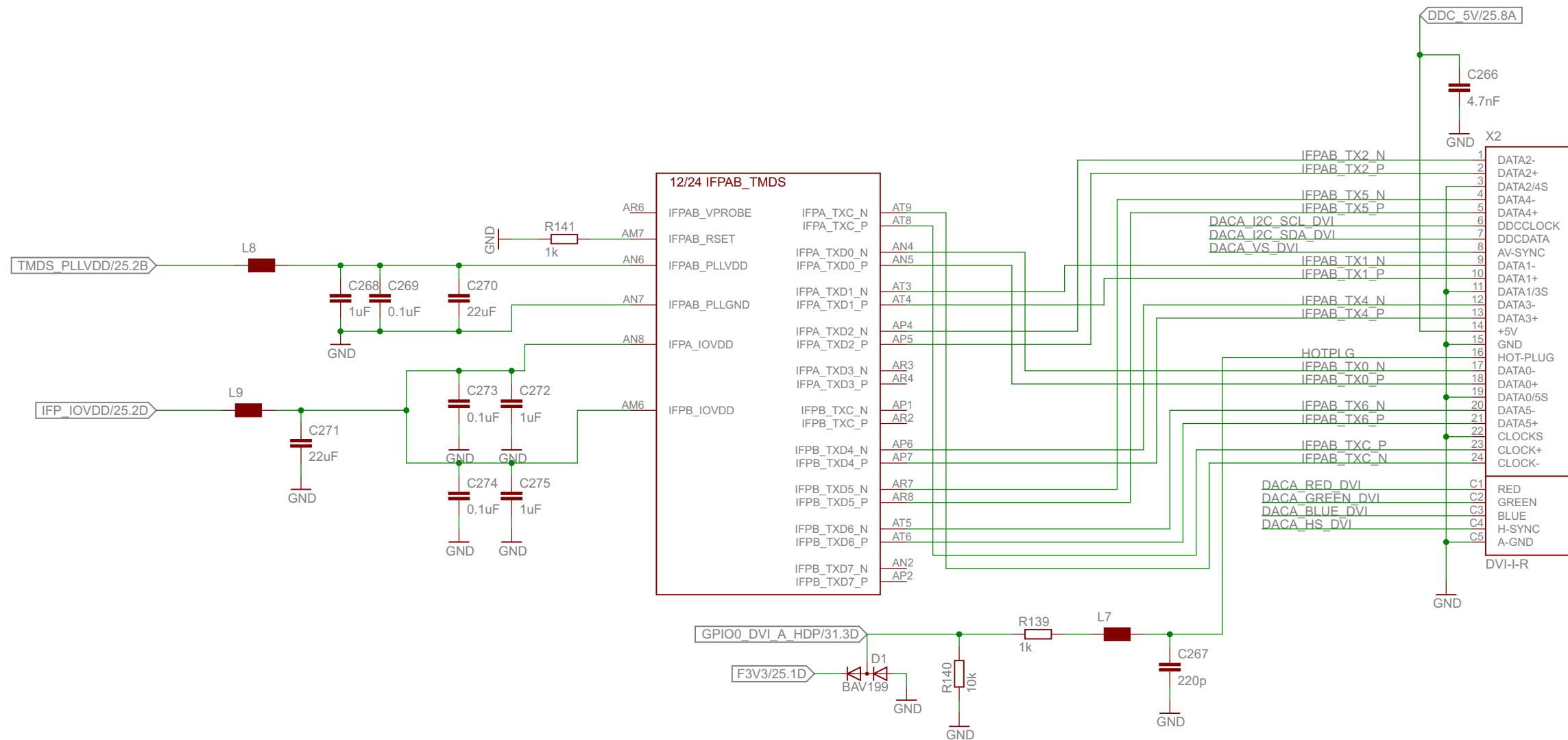
# FBD-HIGH32B-Power



**DUDA**

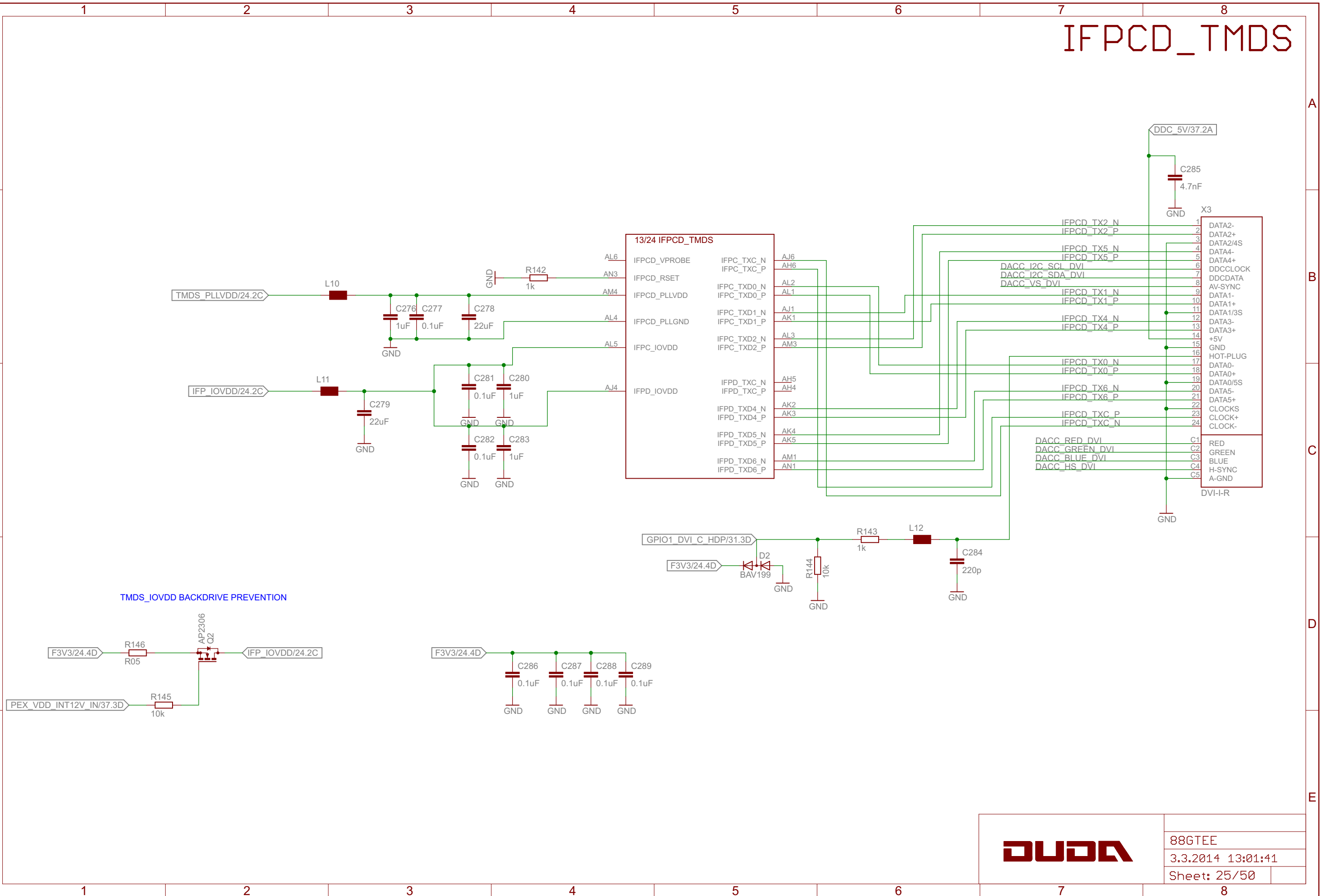
88GTEE  
3.3.2014 13:01:41  
Sheet: 23/50

# IFPAB\_TMDS

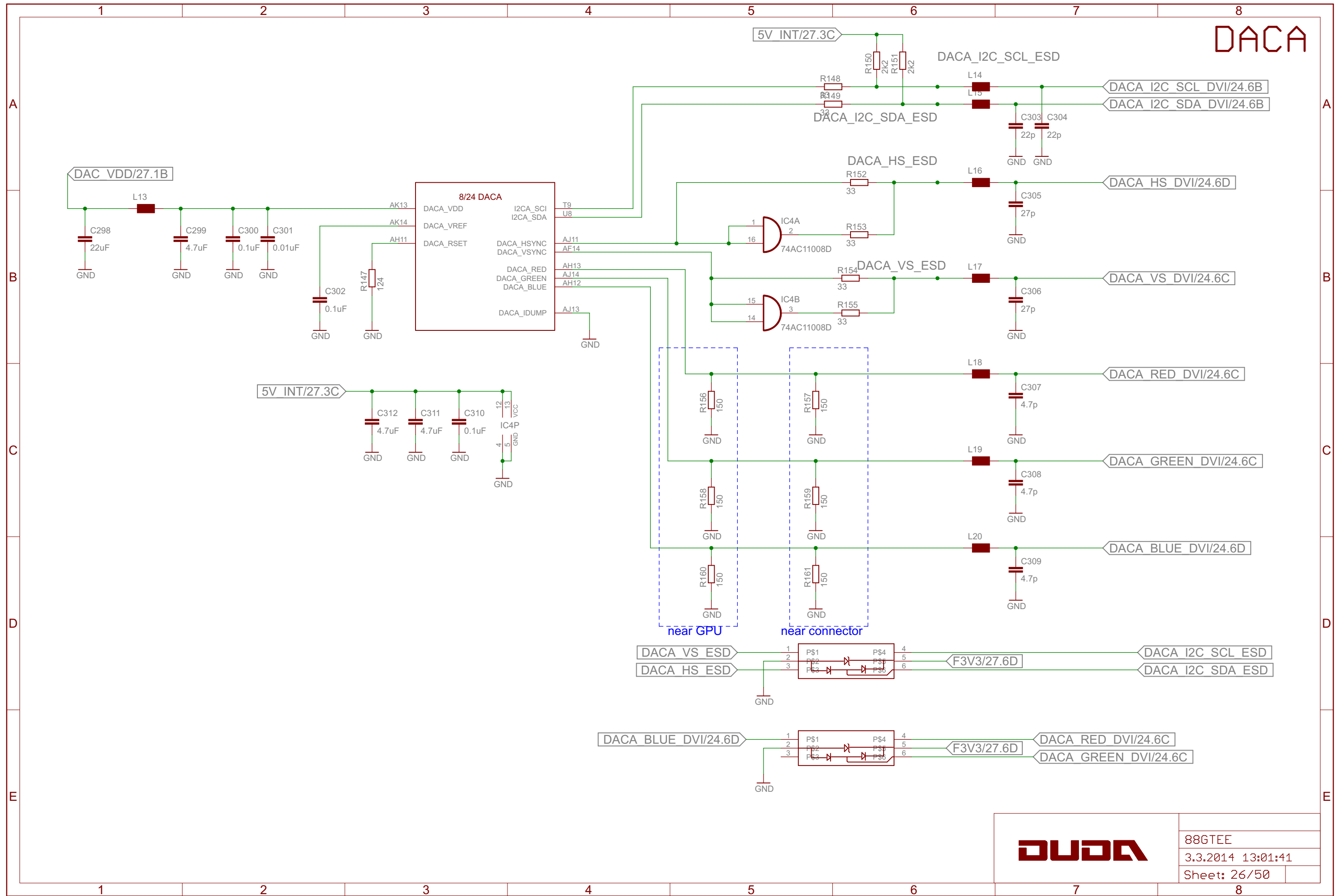


88GTEE  
 3.3.2014 13:01:41  
 Sheet: 24/50

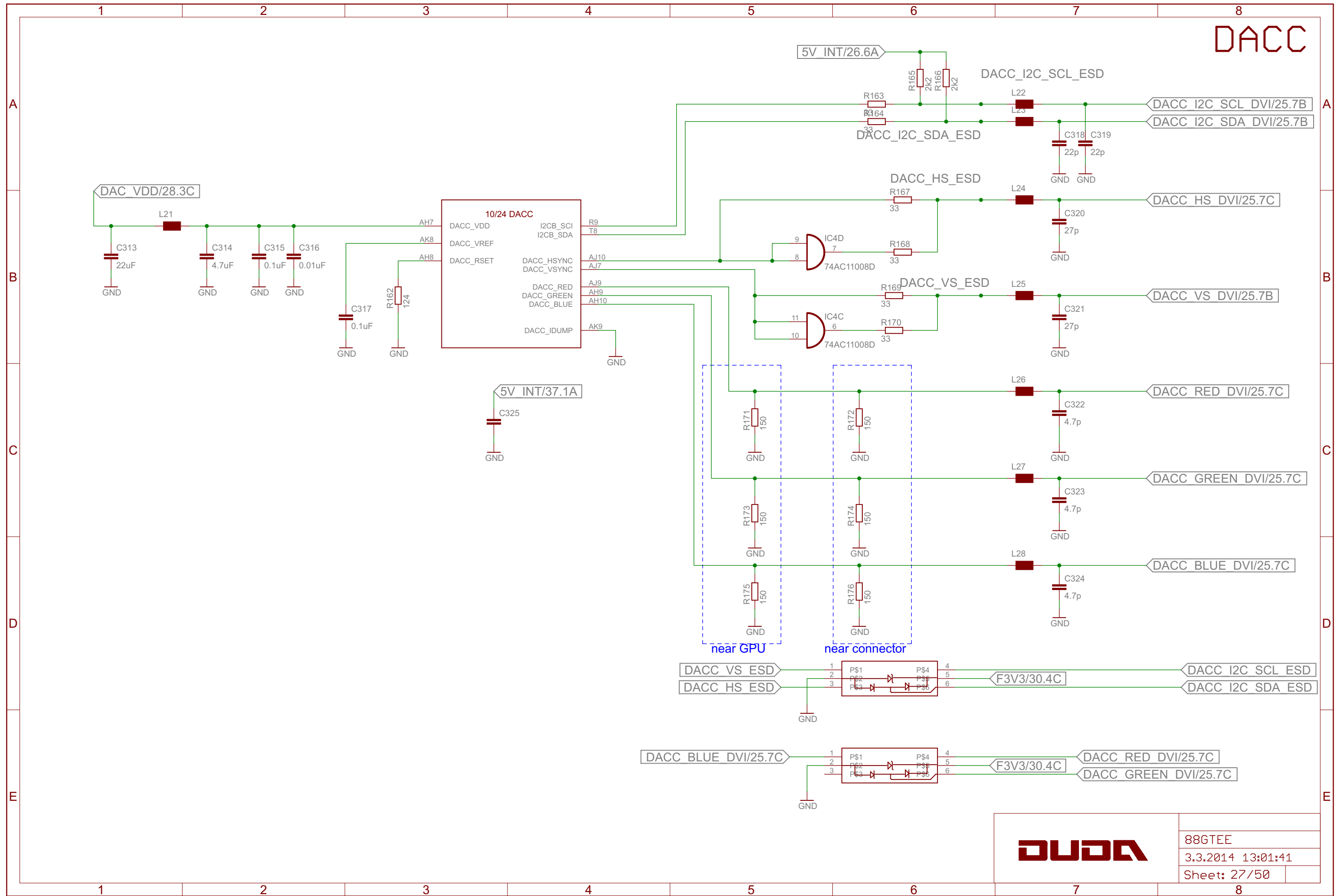
# IFPCD\_TMDS



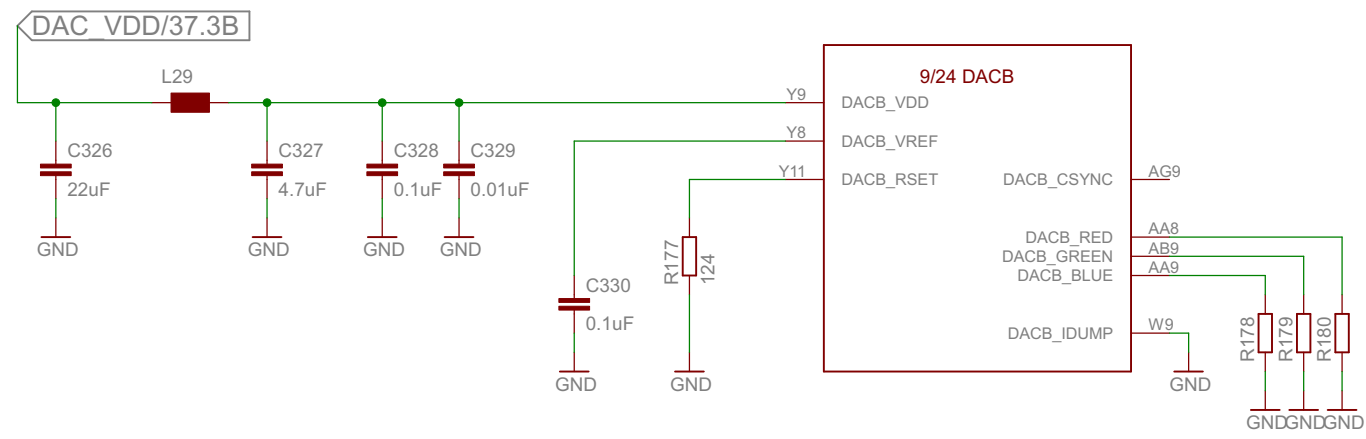
# DACA



# DACC



# DACB

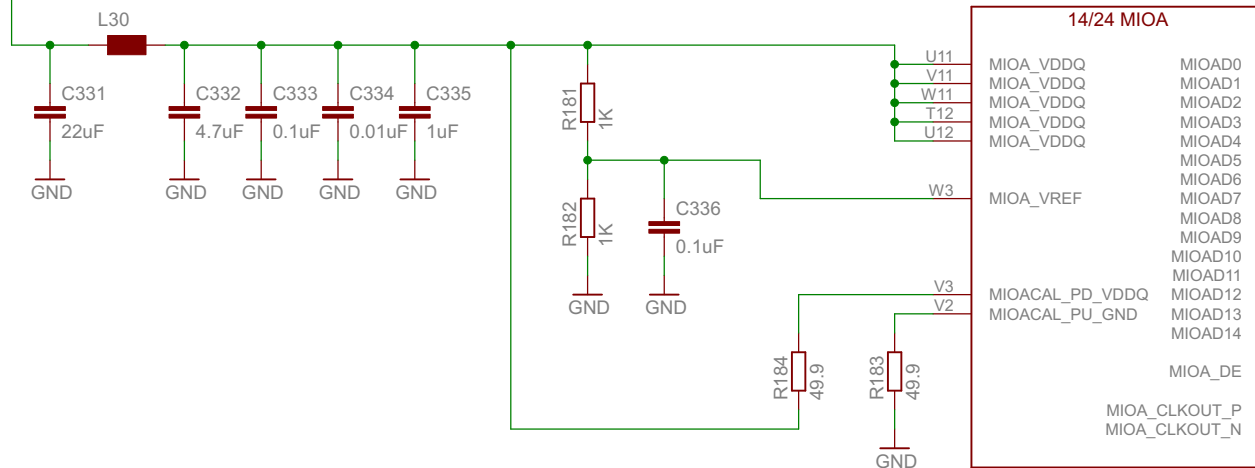


DACB TVOUT NOT USED

# MIOA/MIOB

route on inner layer

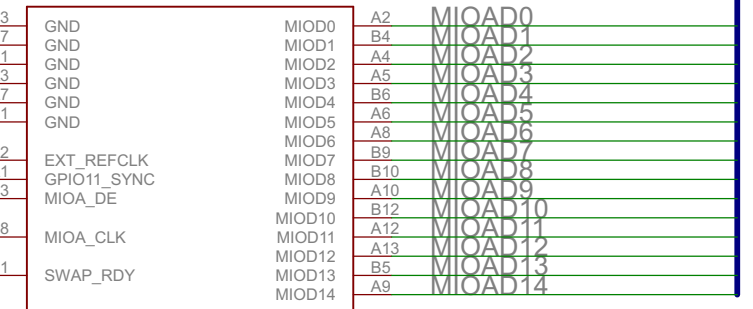
MIOA 2V5/32.4A



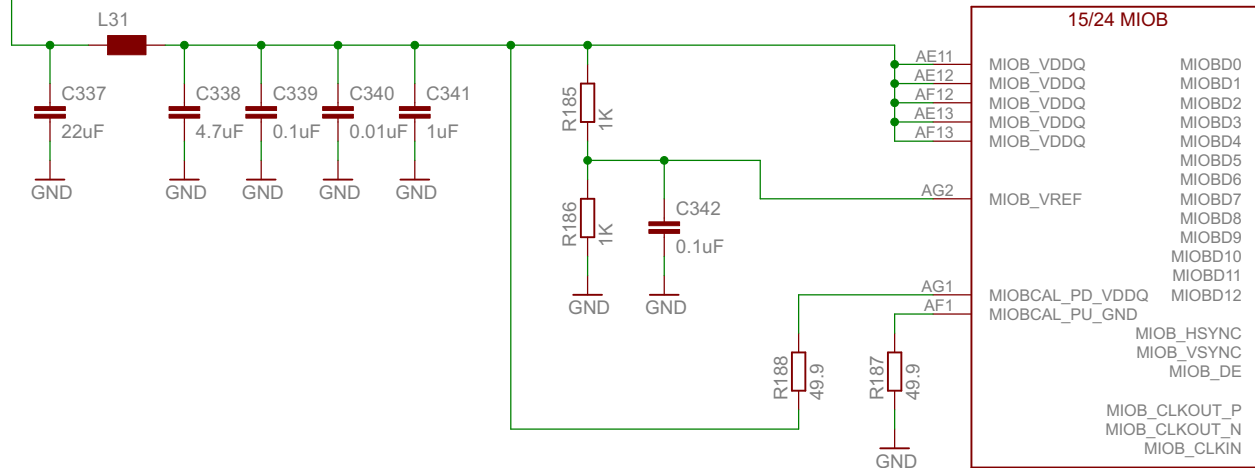
MIOAD[0..14]

GPIO11 SYNC/31.3E

SWAPRDY A/31.4C



MIOA 2V5/32.4A



MIOBD[0..12]

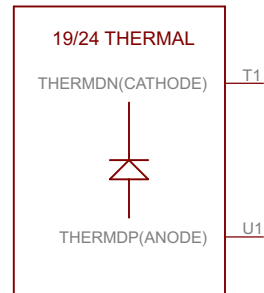


88GTEE  
3.3.2014 13:01:41  
Sheet: 29/50

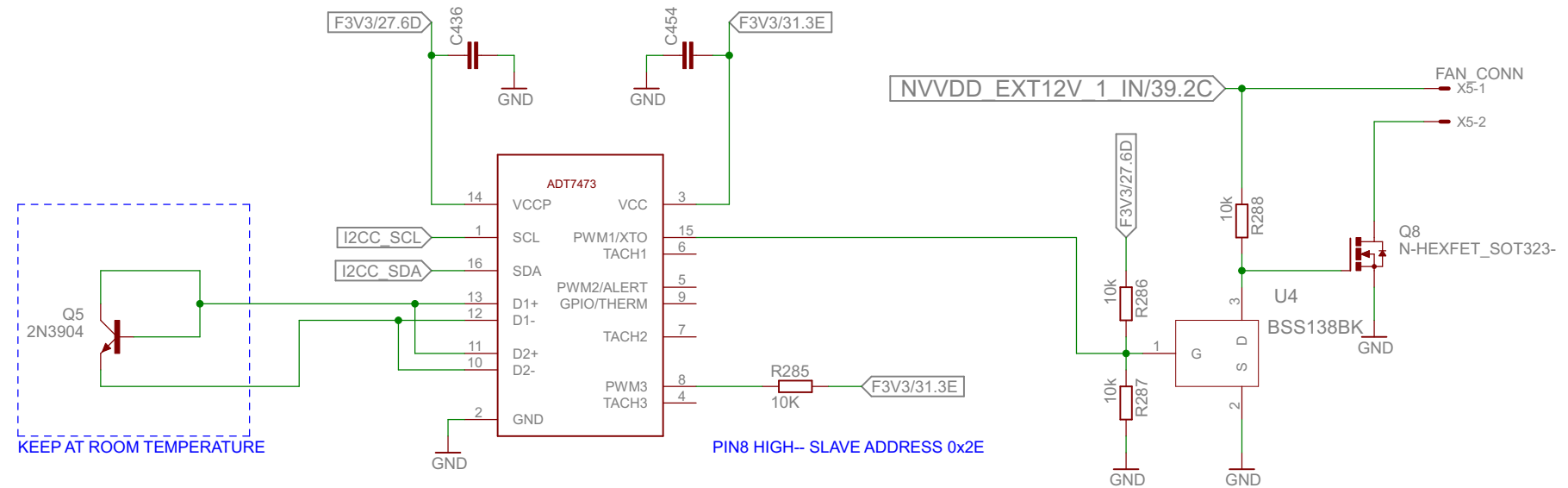


# XTAL/THERM/FAN/I2C/HDCP

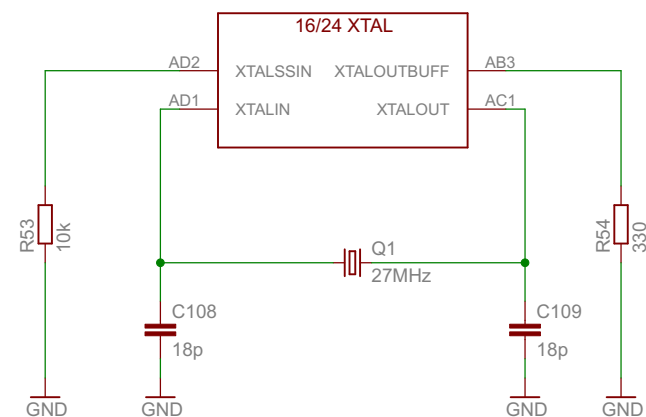
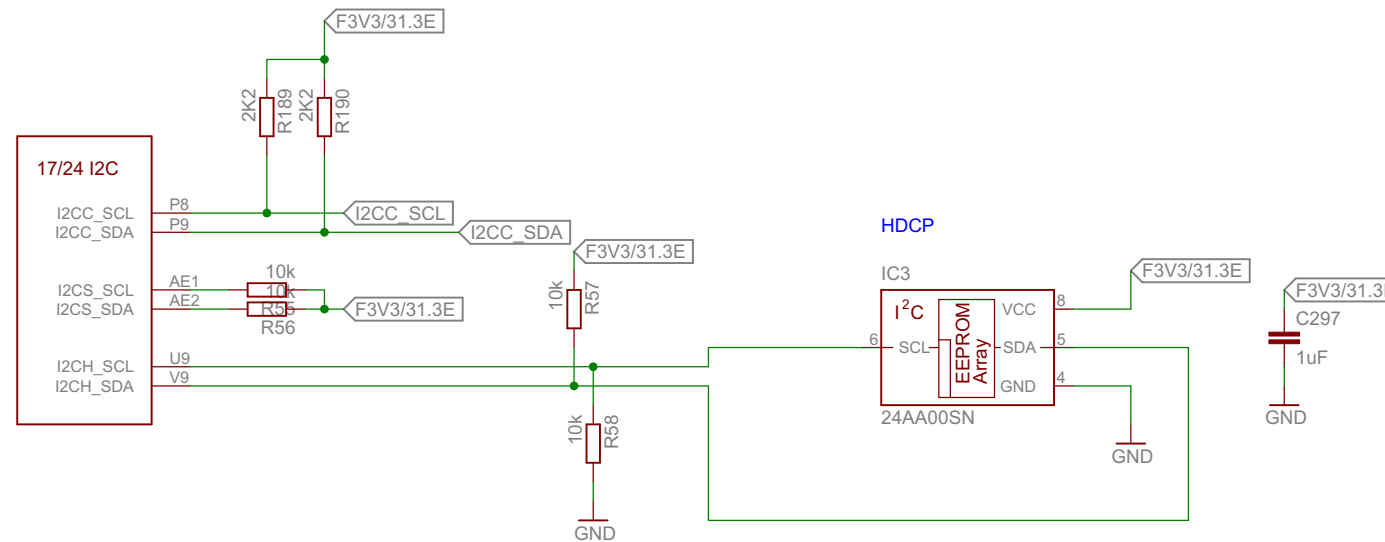
NO INTERNAL THERMAL MONITORING



KEEP AT ROOM TEMPERATURE



PIN8 HIGH-- SLAVE ADDRESS 0x2E



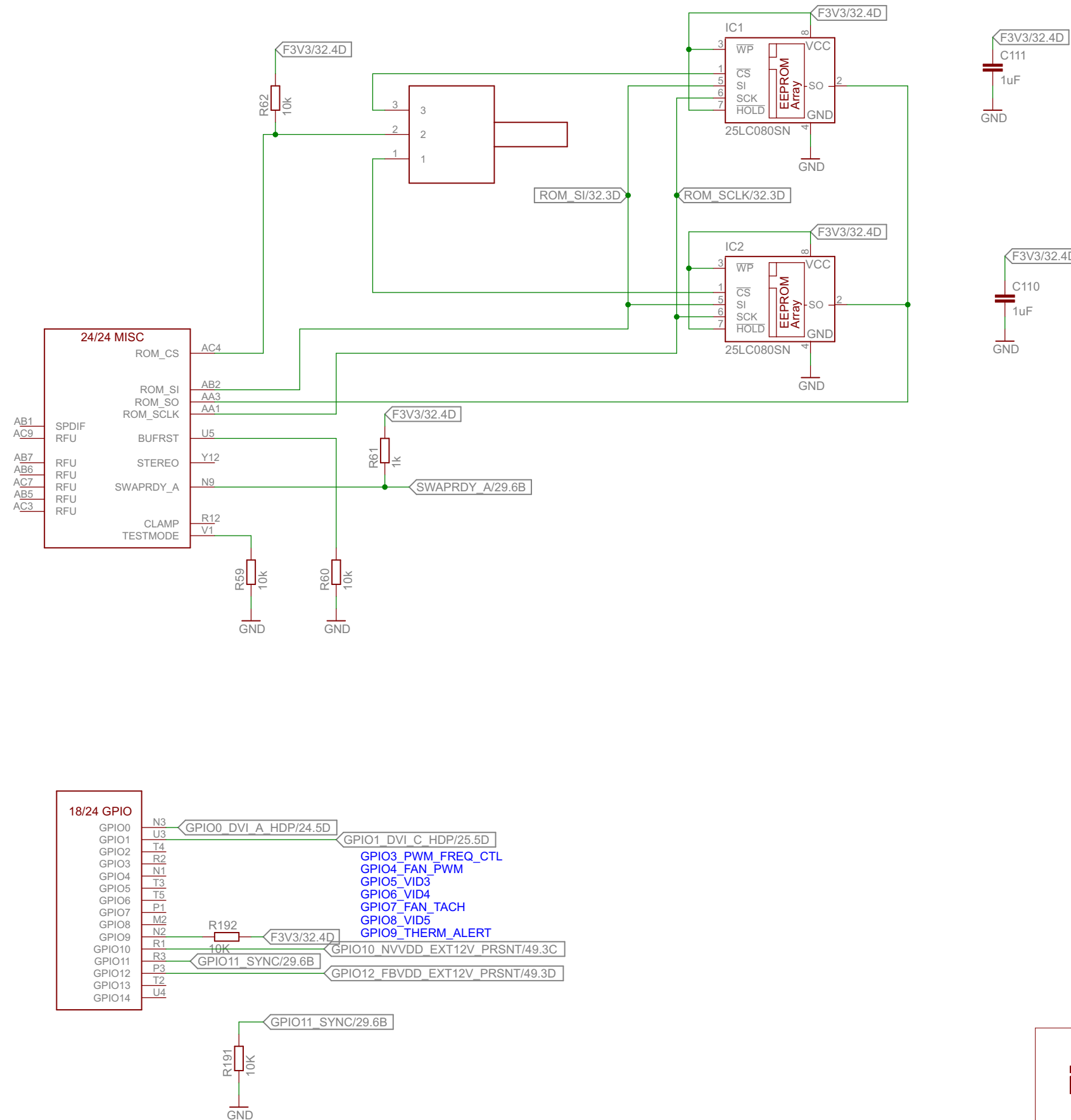
R(53-56)--5%

C(108-109)--NPO/50V/5%

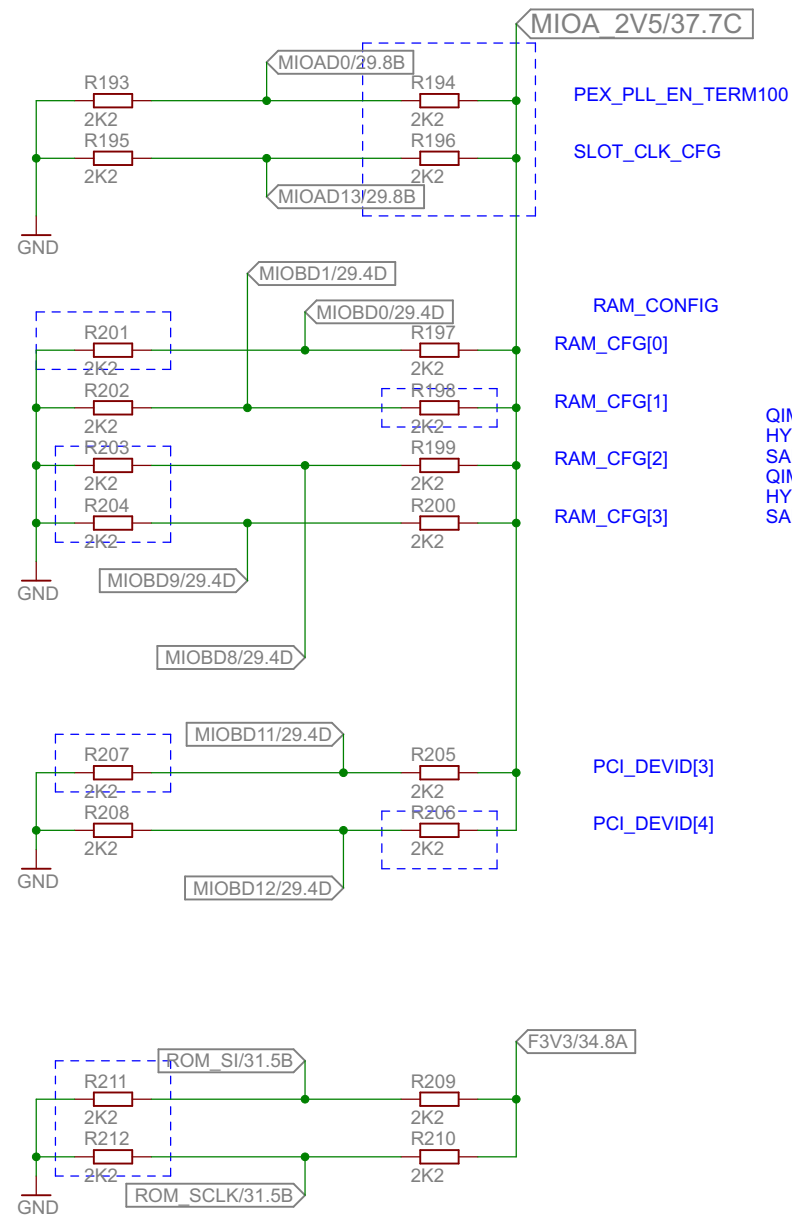


88GTEE  
3.3.2014 13:01:41  
Sheet: 30/50

# BIOS/GPIO



# STRAP CONFIG

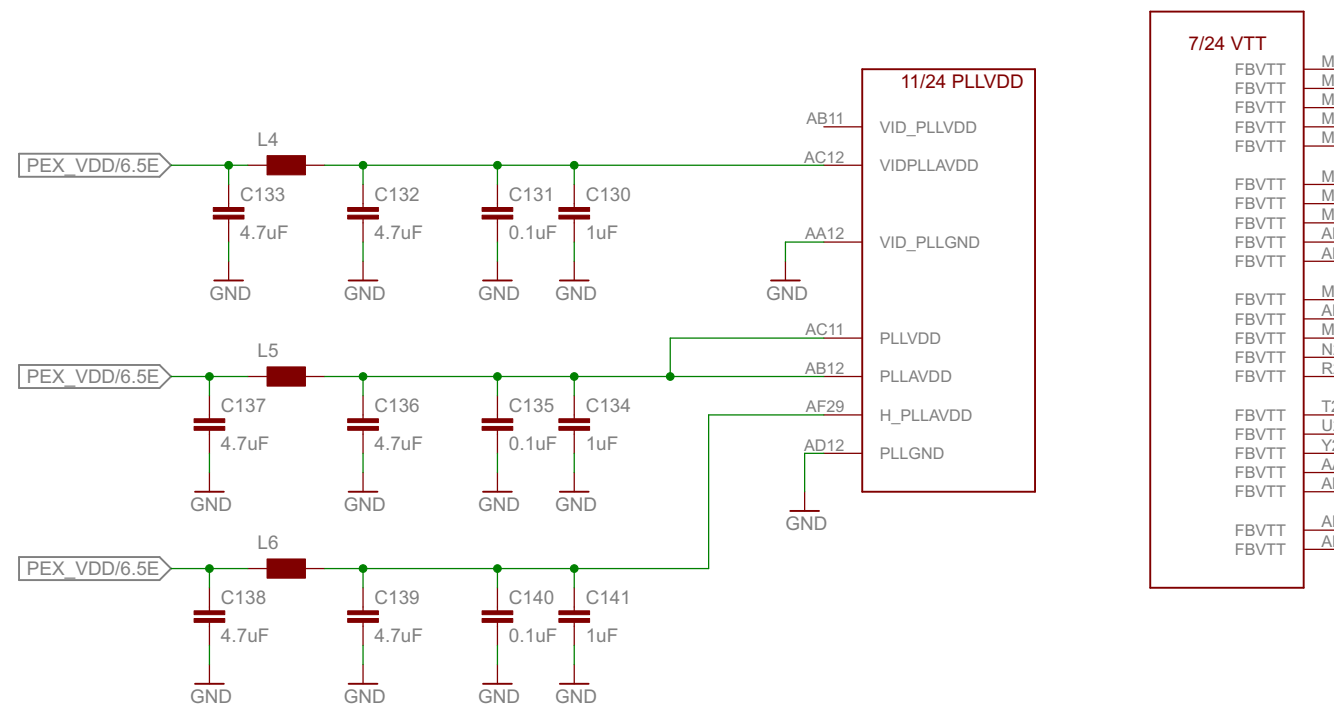


QIMONDA 16MX32 0001  
 HYNIX 16MX32 0010  
 SAMSUNG 16MX32 0011  
 QIMONDA 8MX32 0100  
 HYNIX 8MX32 0110  
 SAMSUNG 8MX32 0111



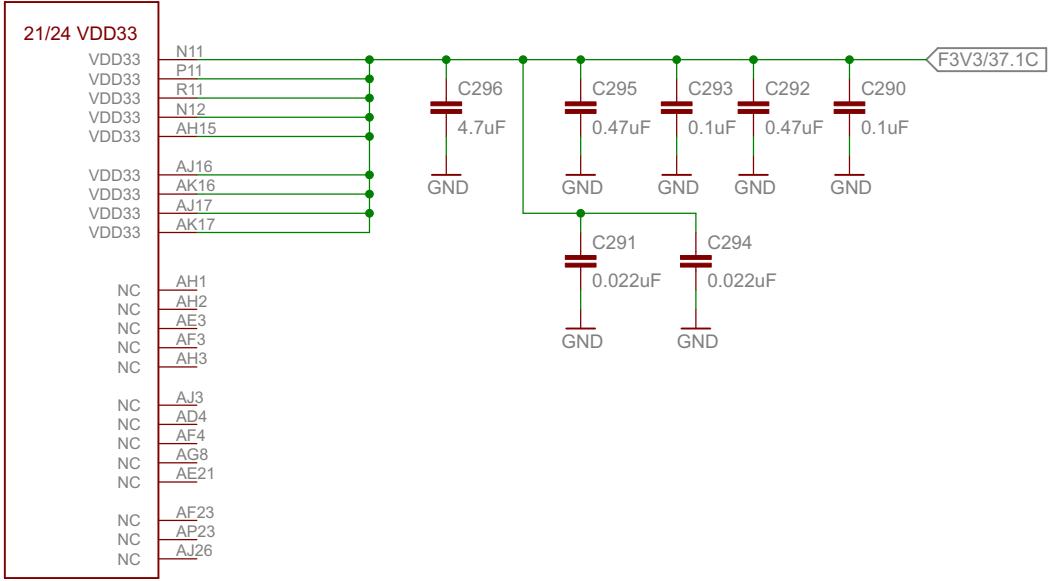
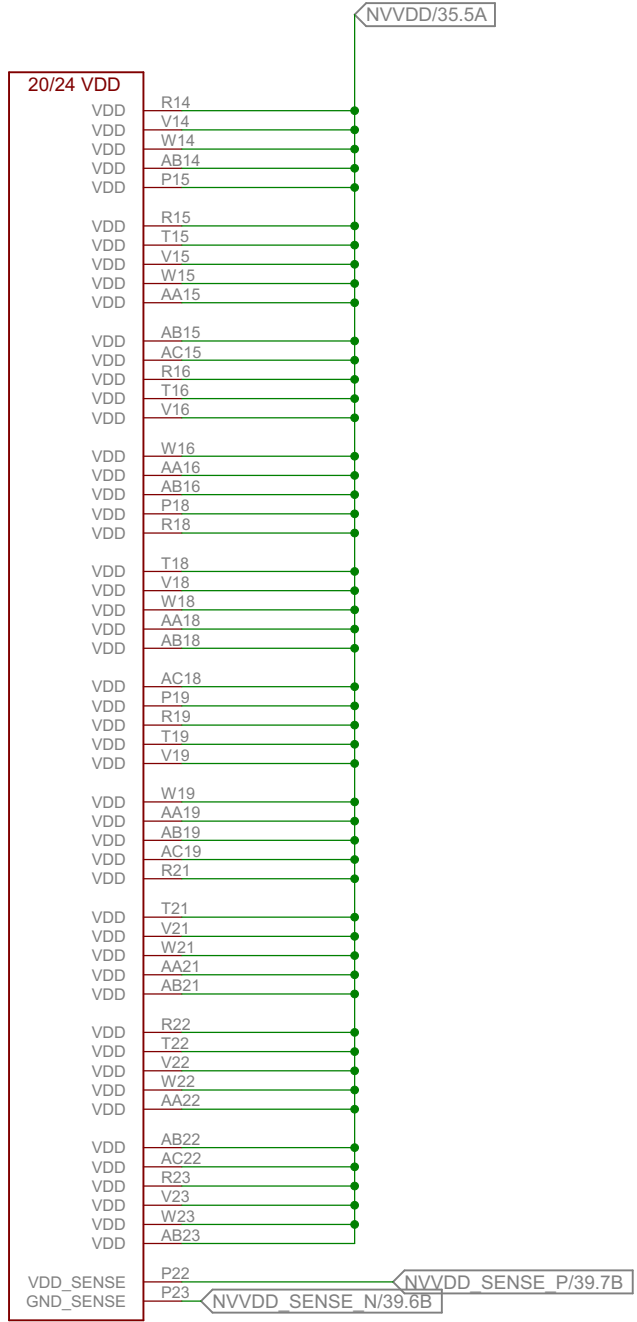
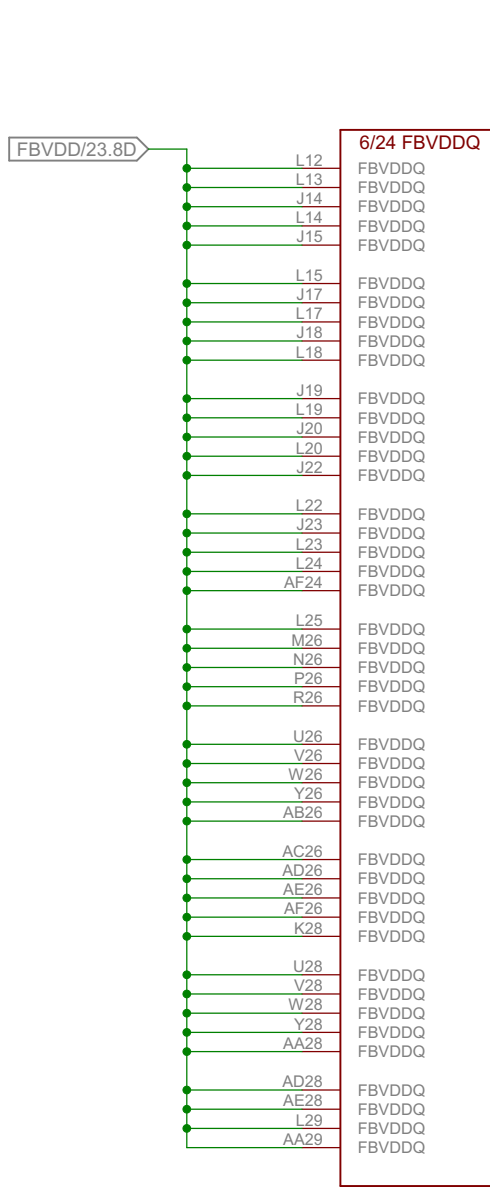
88GTEE  
 3.3.2014 13:01:41  
 Sheet: 32/50

# PLL VDD/VTT

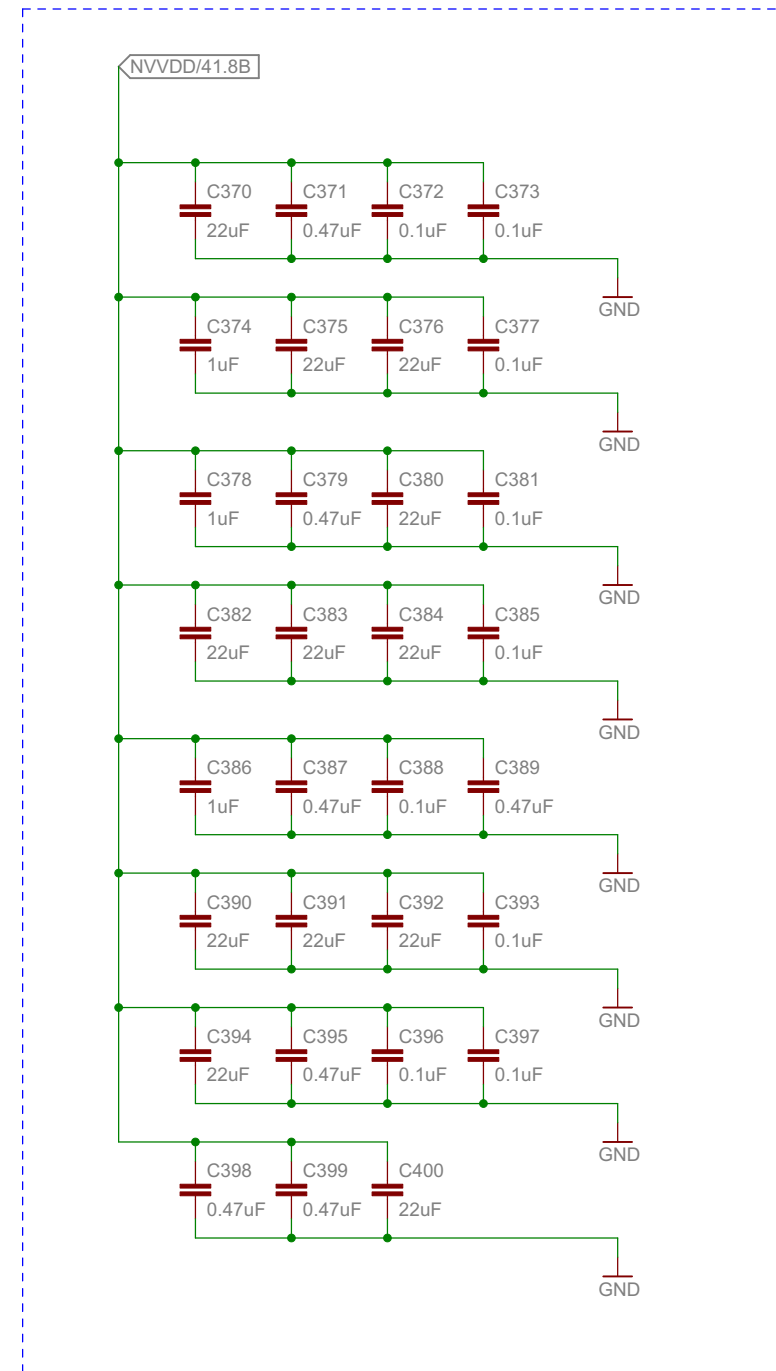
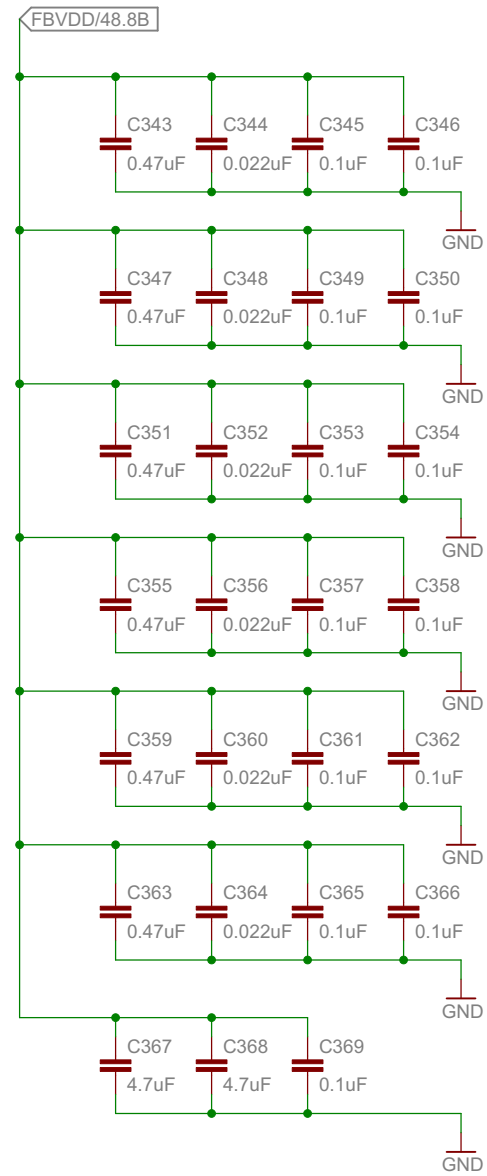


7/24 VTT	
FBVTT	M12
FBVTT	M13
FBVTT	M15
FBVTT	M16
FBVTT	M17
FBVTT	M20
FBVTT	M21
FBVTT	M22
FBVTT	AE22
FBVTT	AE23
FBVTT	M24
FBVTT	AE24
FBVTT	M25
FBVTT	N25
FBVTT	R25
FBVTT	T25
FBVTT	U25
FBVTT	Y25
FBVTT	AA25
FBVTT	AB25
FBVTT	AD25
FBVTT	AE25

# NVVDD/VDD33/FBVDDQ

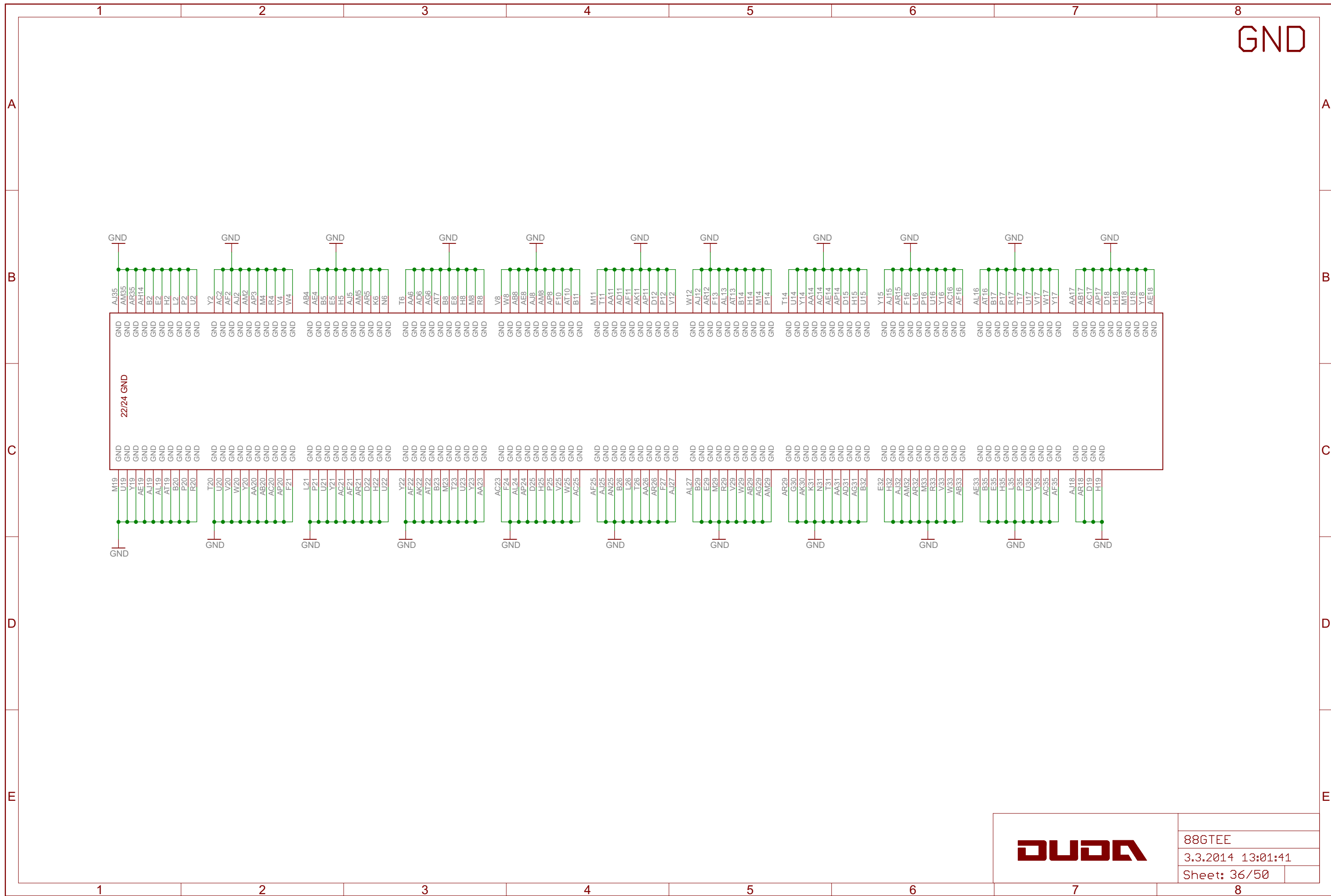


# DECOUPLING NVVDD/FBVDD

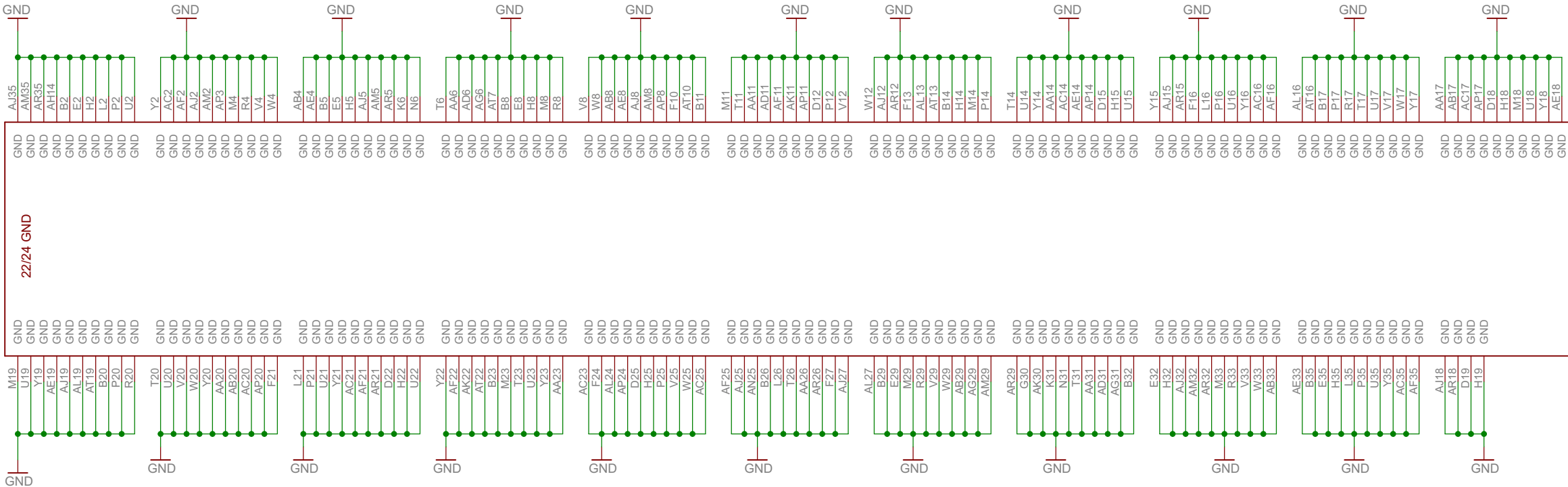


PLACE UNDER GPU!

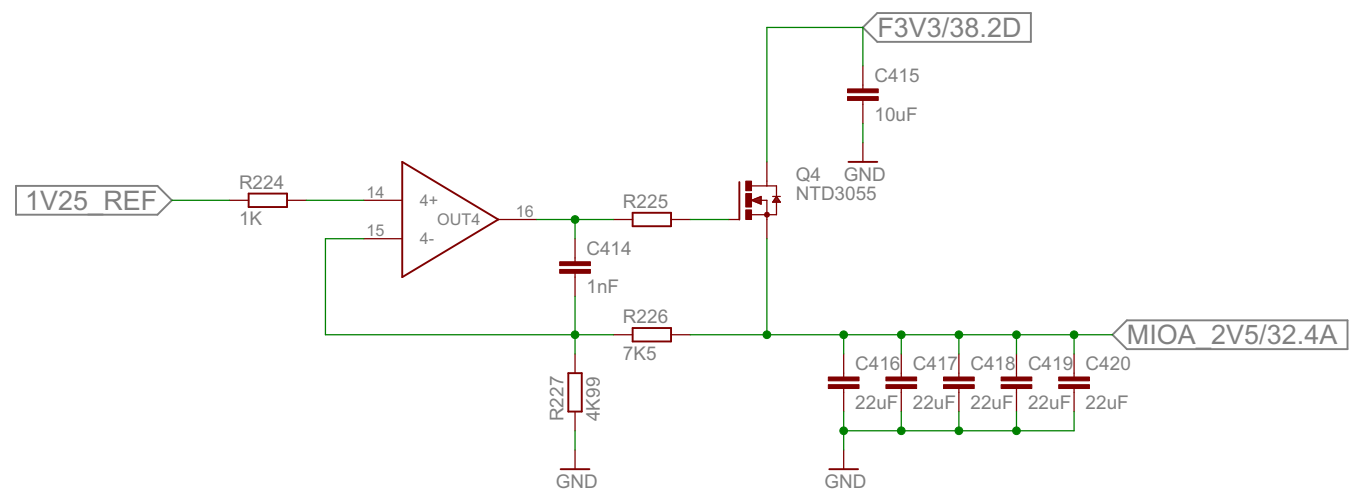
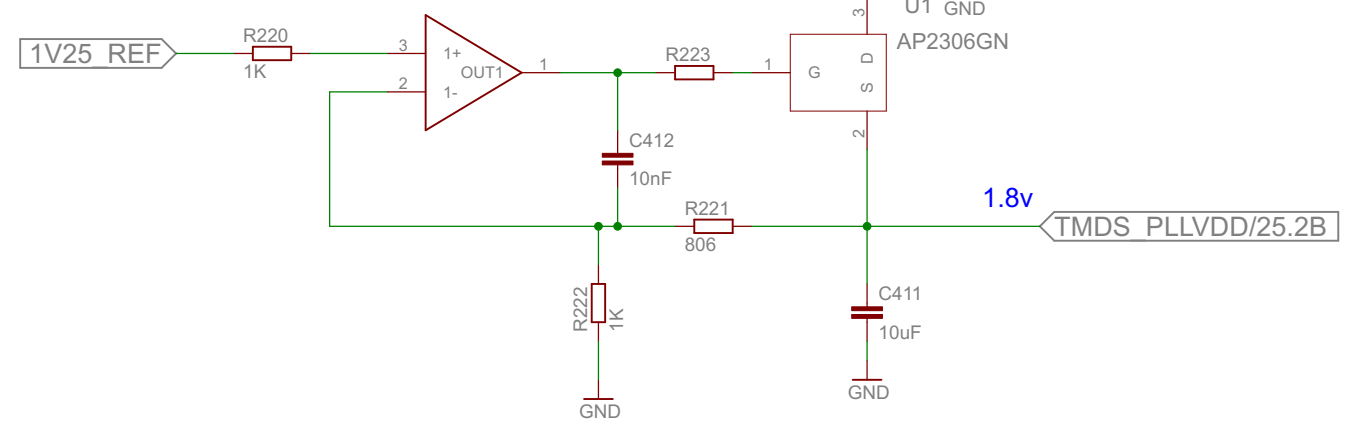
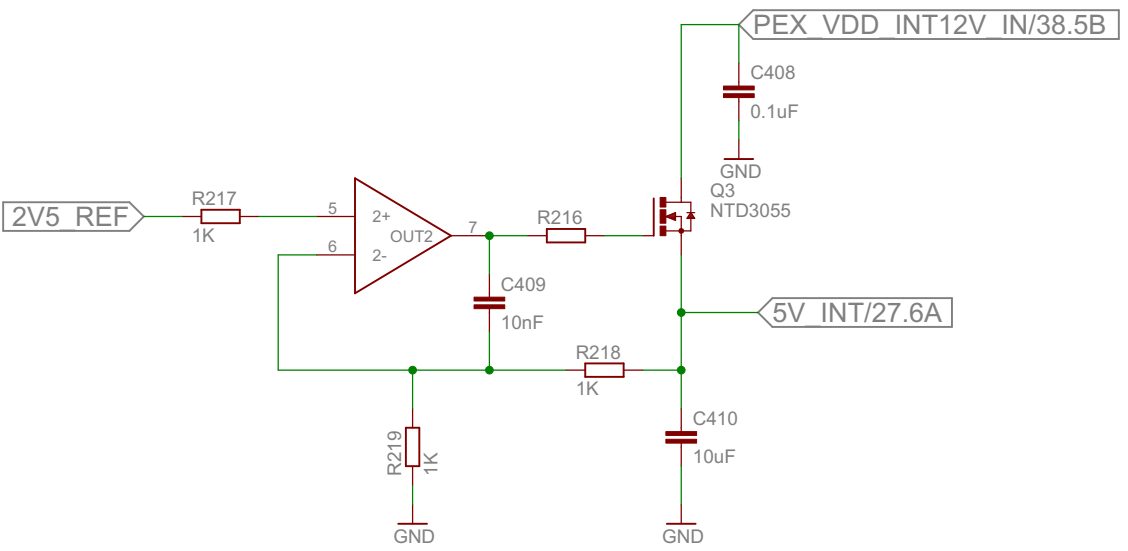
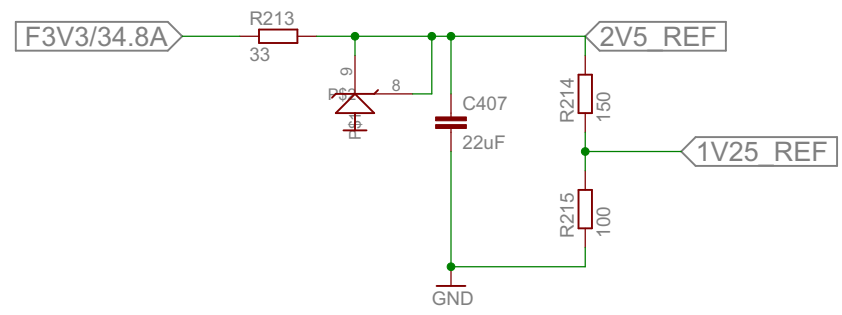
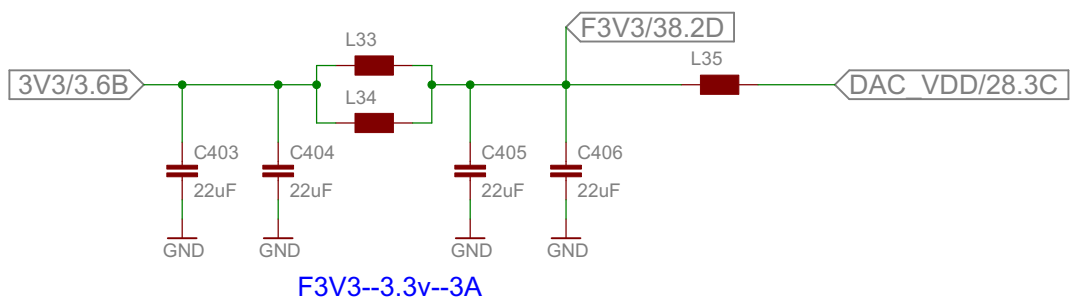
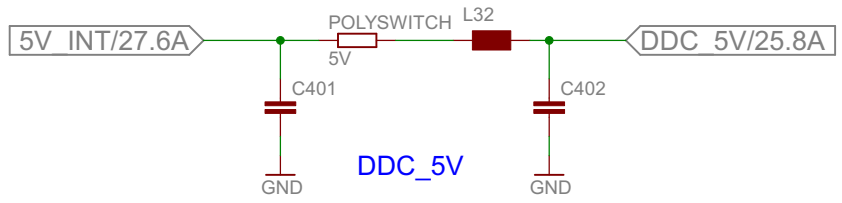




GND

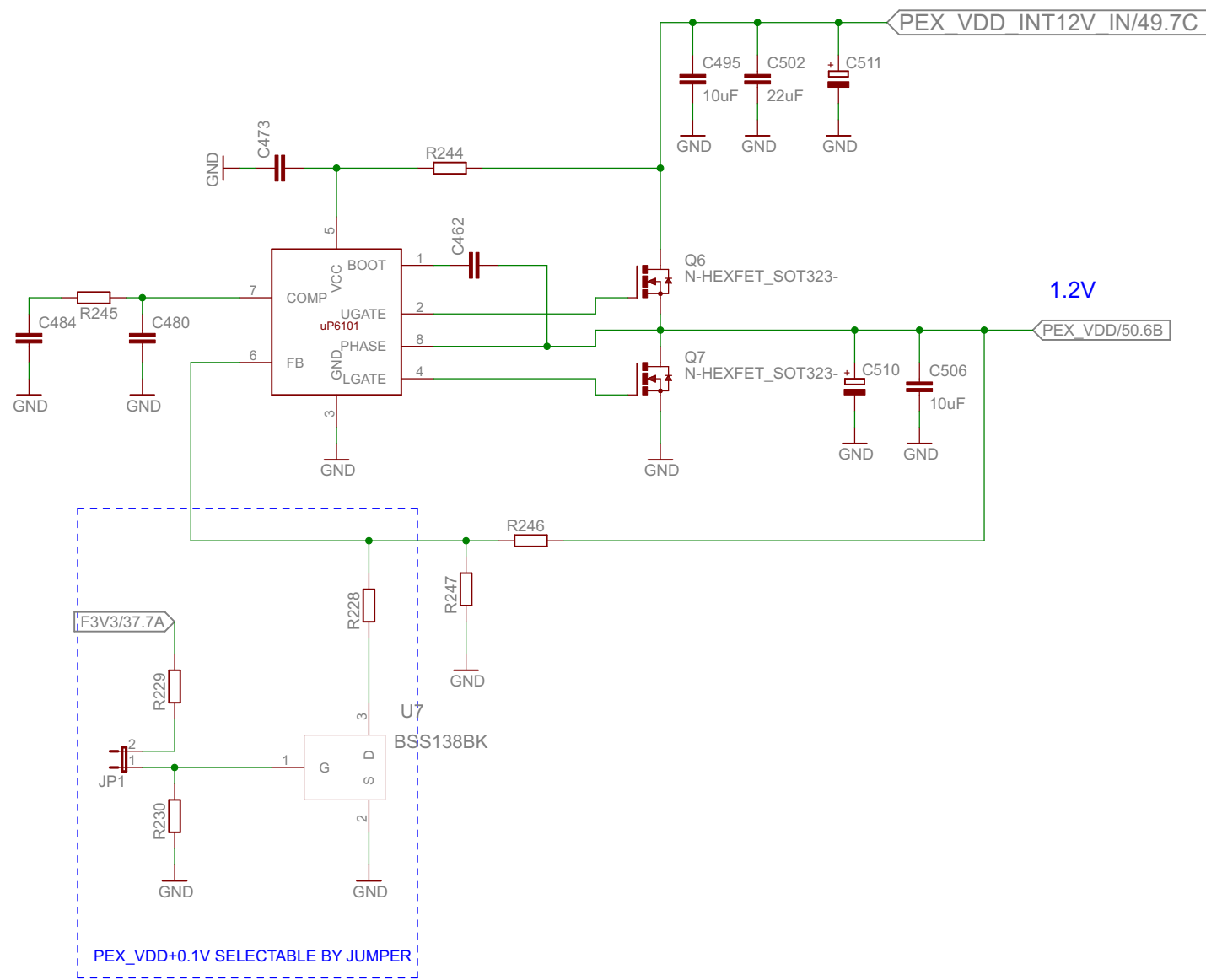


# SUPPLY DAC\_VDD/5V\_INT/TMDS\_PLLVDD/MIOA\_2V5

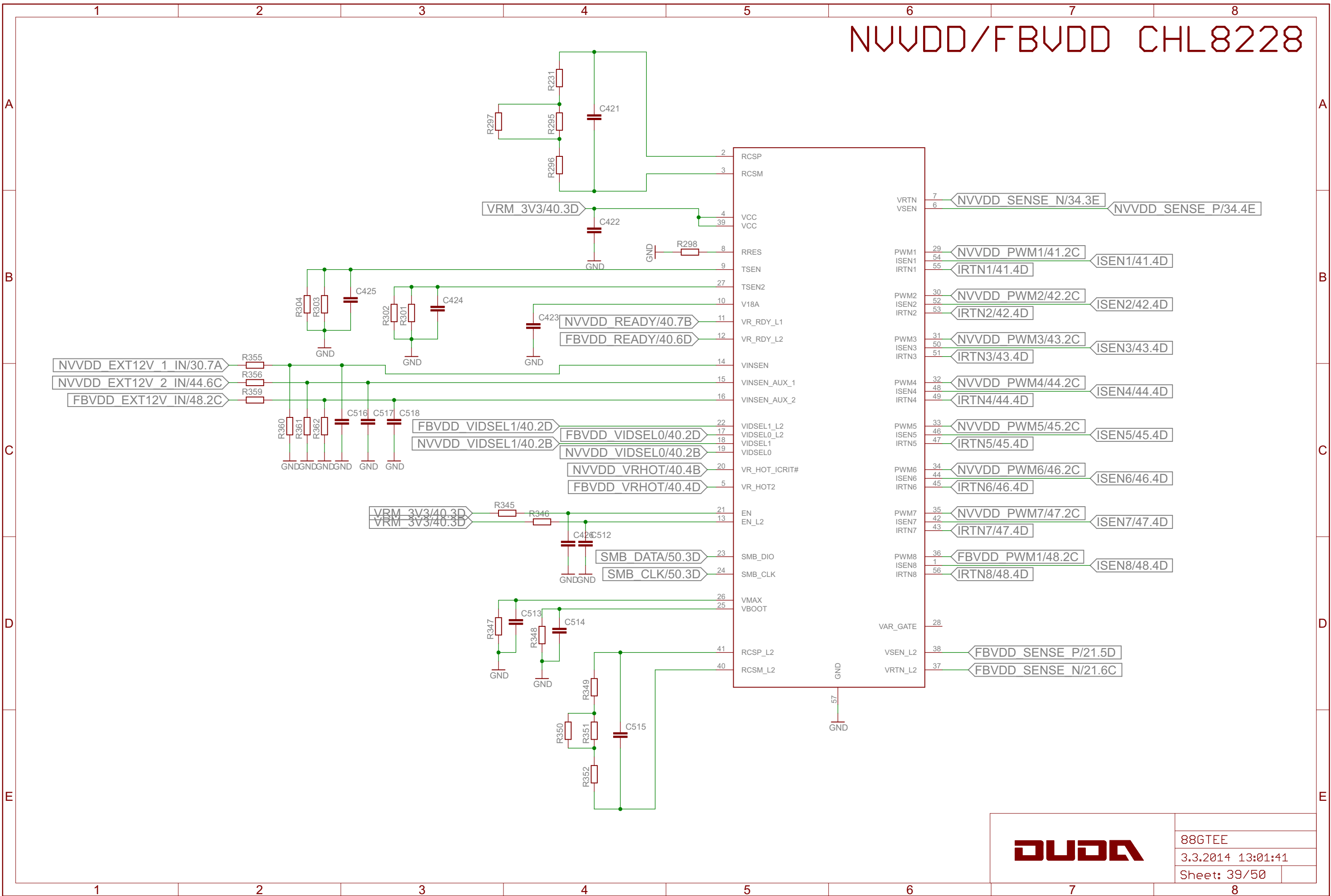




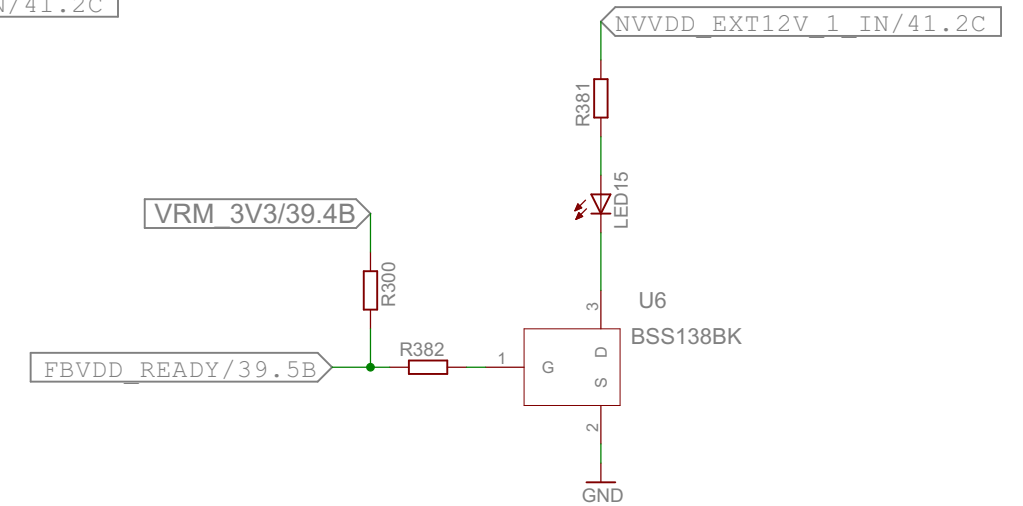
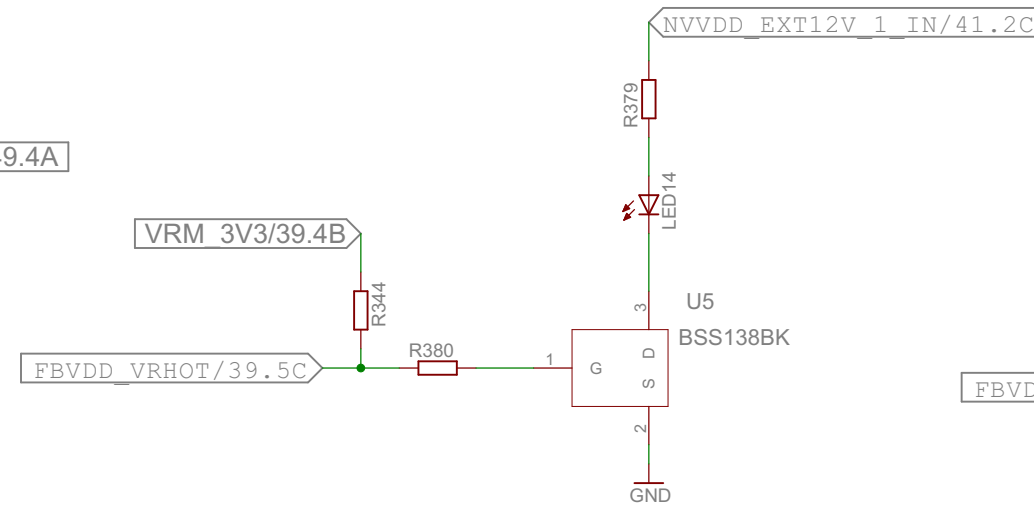
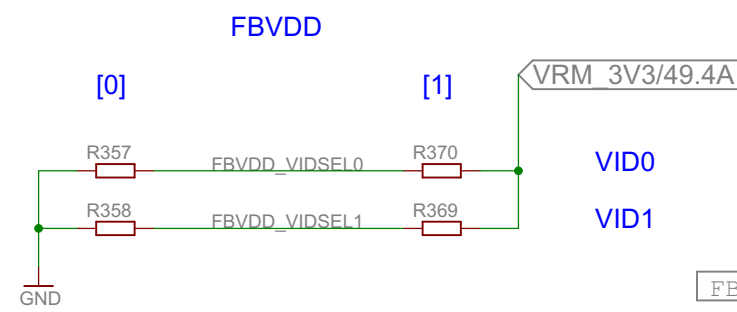
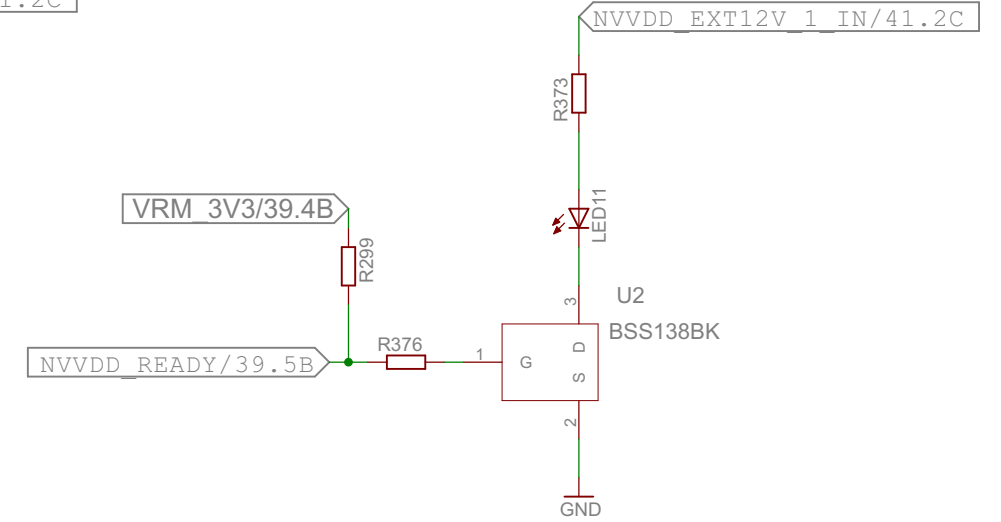
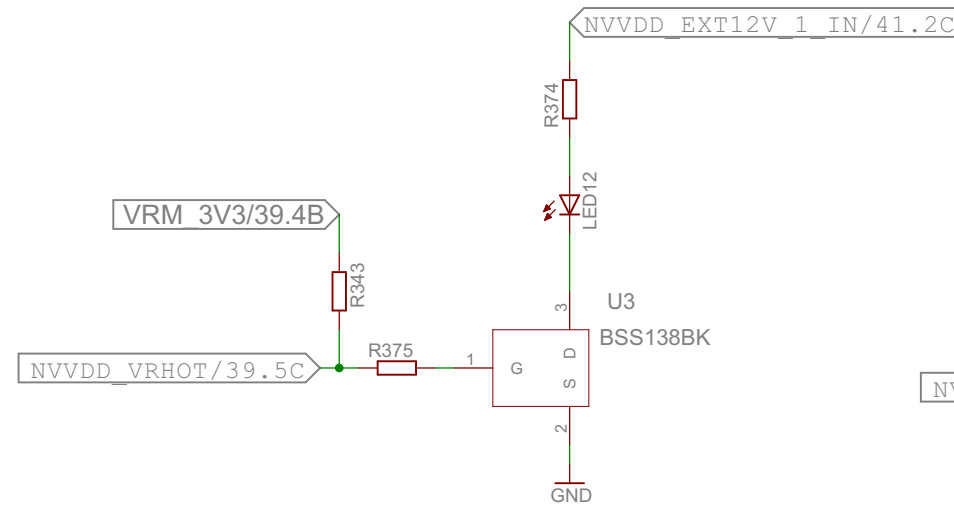
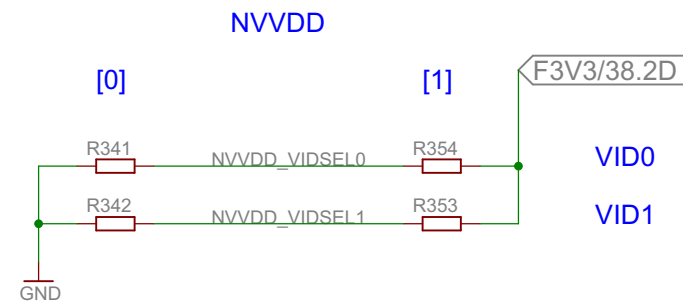
# PEX\_VDD(PLL)



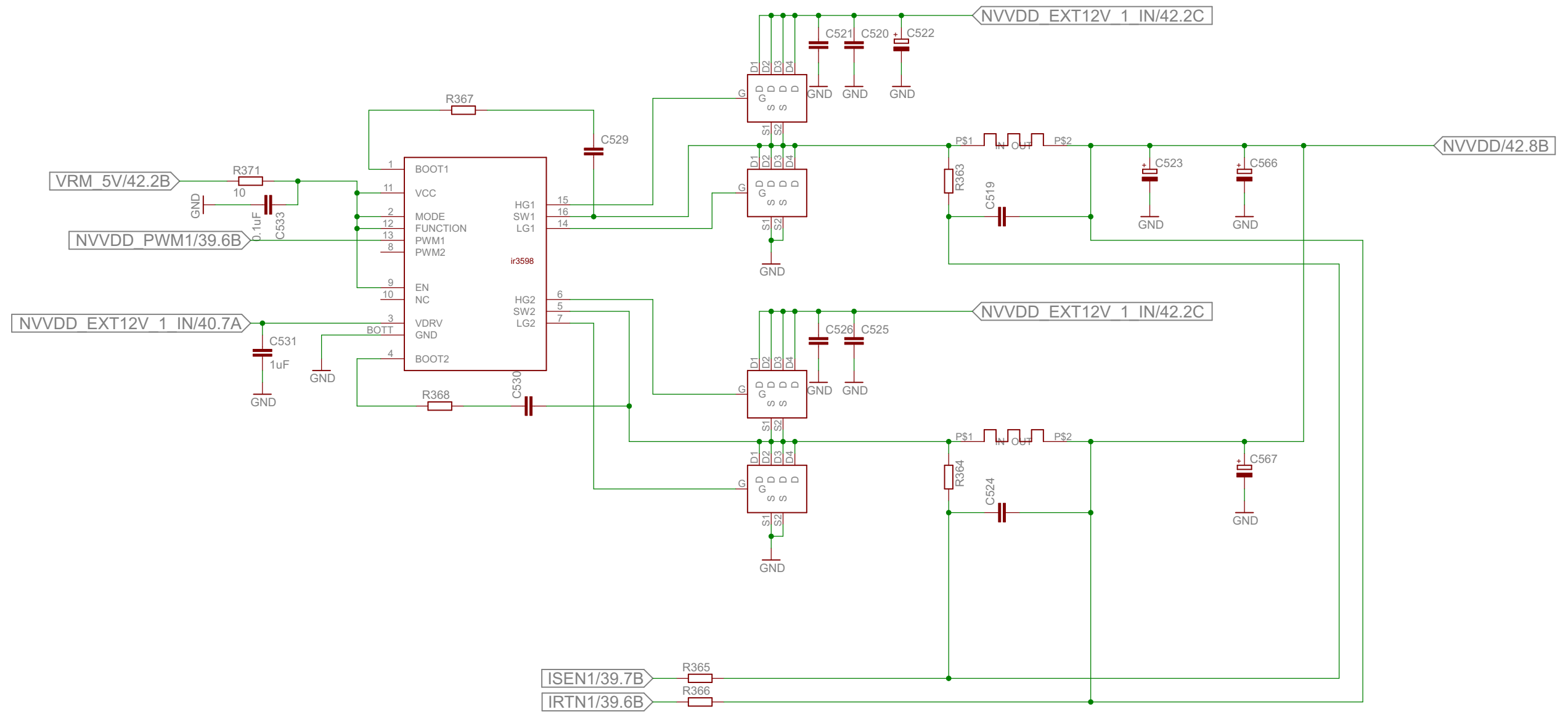
# NVVDD/FBVDD CHL8228



# NVVDD/FBVDD CONFIG

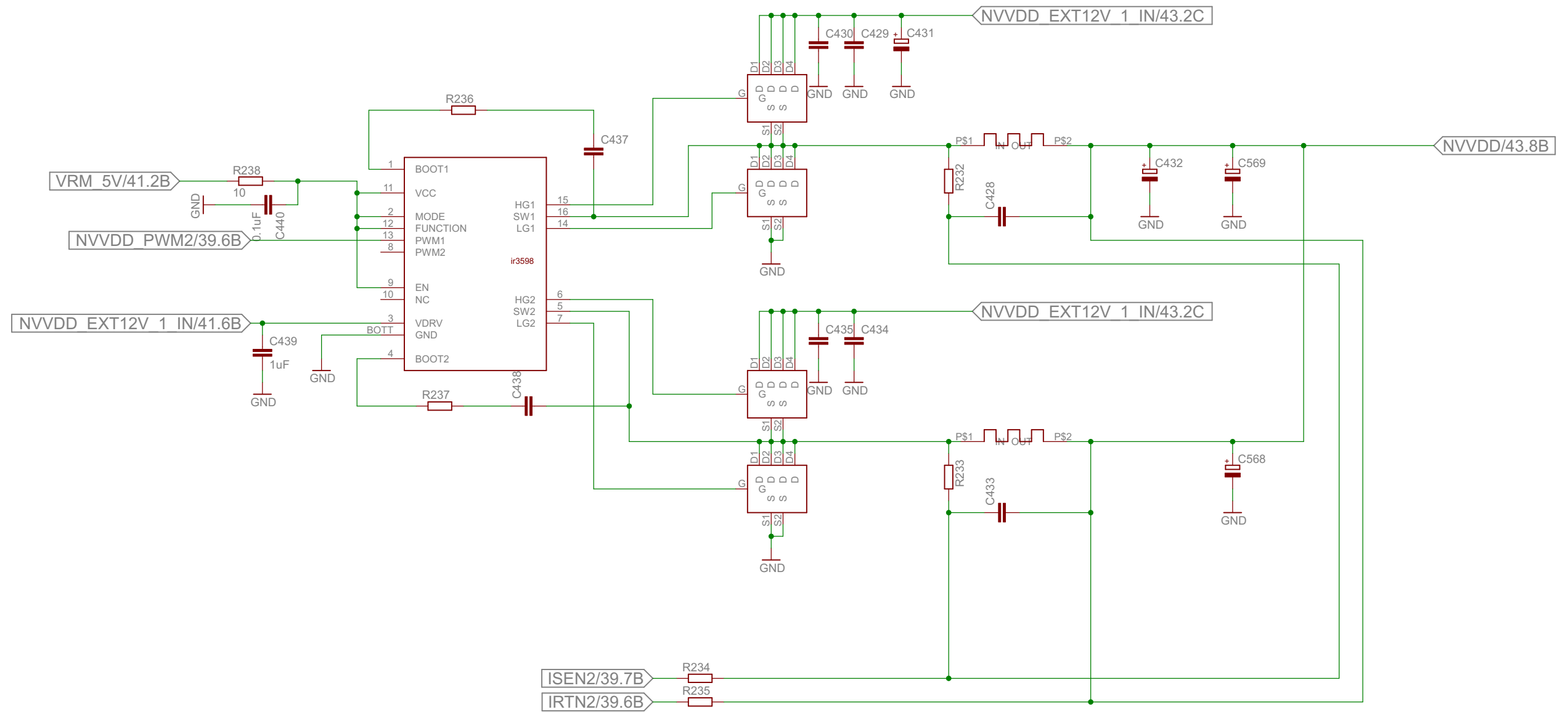


# NVVDD\_PHASE\_1-2



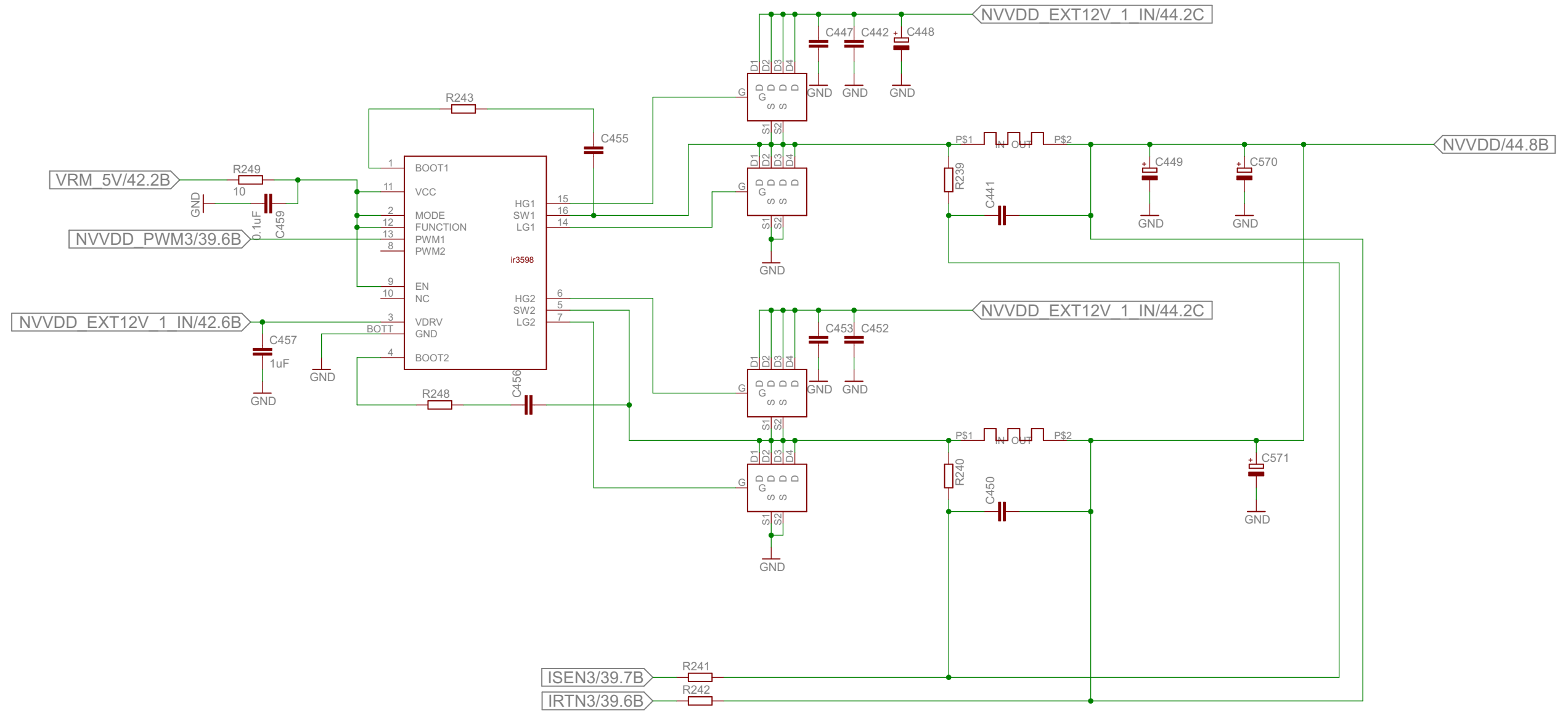
88GTEE  
 3.3.2014 13:01:41  
 Sheet: 41/50

# NVVDD\_PHASE\_3-4



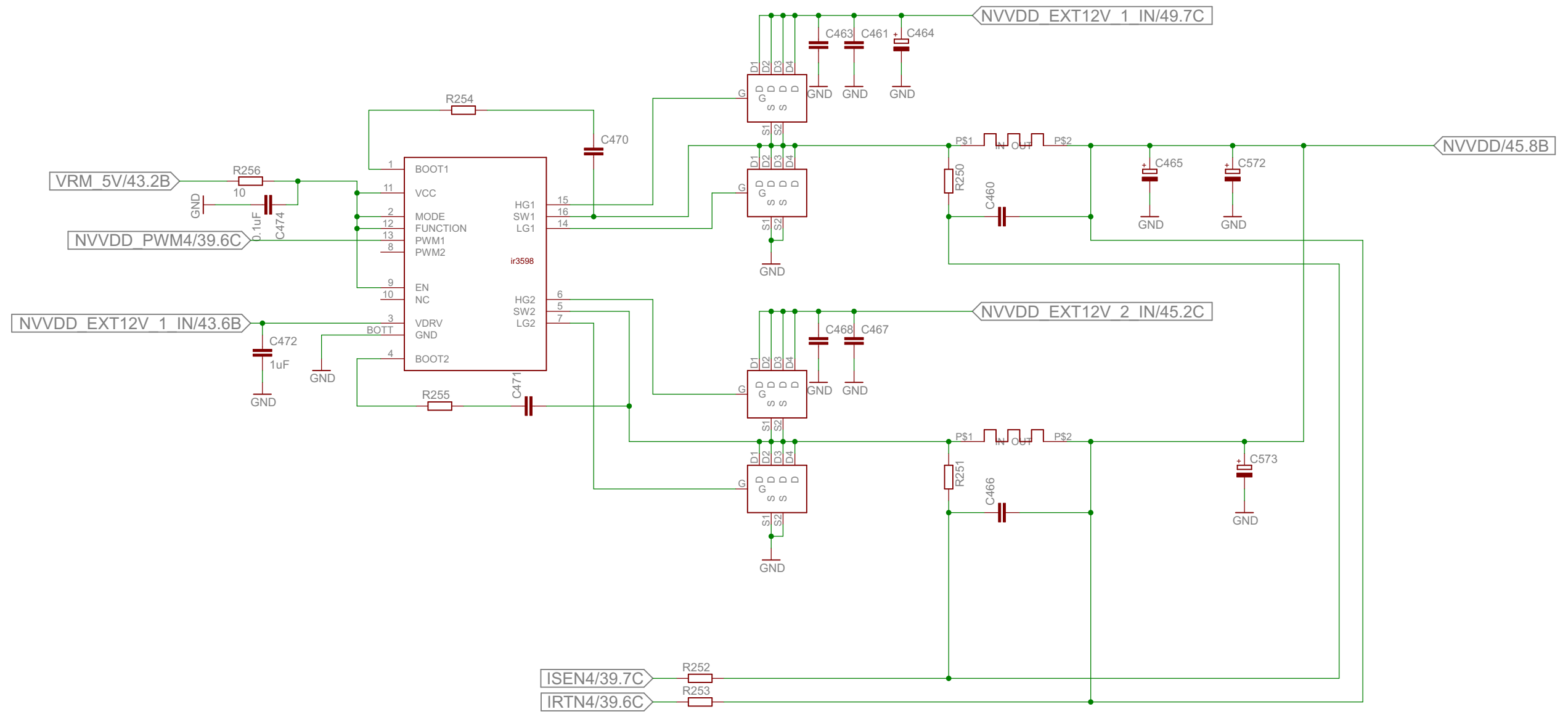
88GTEE  
 3.3.2014 13:01:41  
 Sheet: 42/50

# NVVDD\_PHASE\_5-6



88GTEE  
 3.3.2014 13:01:41  
 Sheet: 43/50

# NVVDD\_PHASE\_7-8

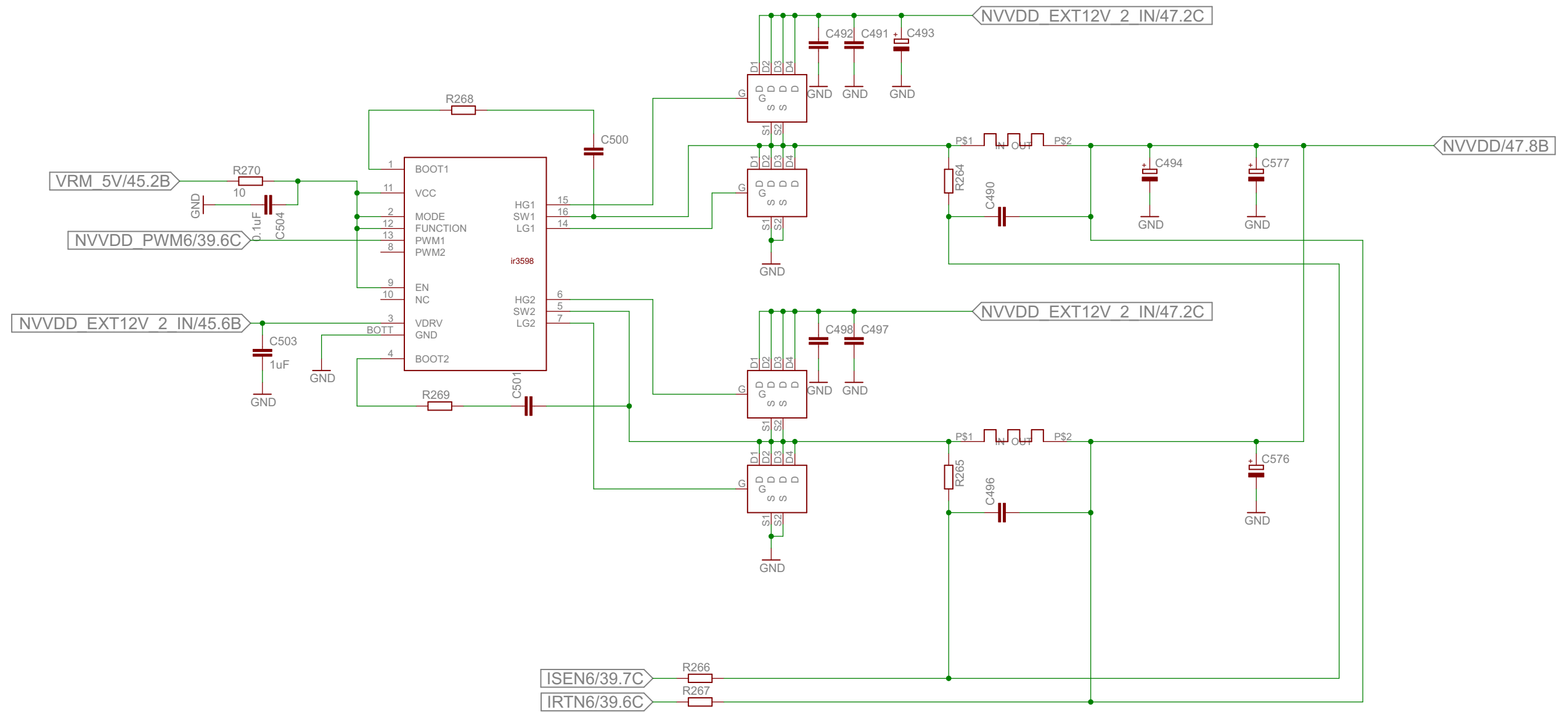


88GTEE  
 3.3.2014 13:01:41  
 Sheet: 44/50



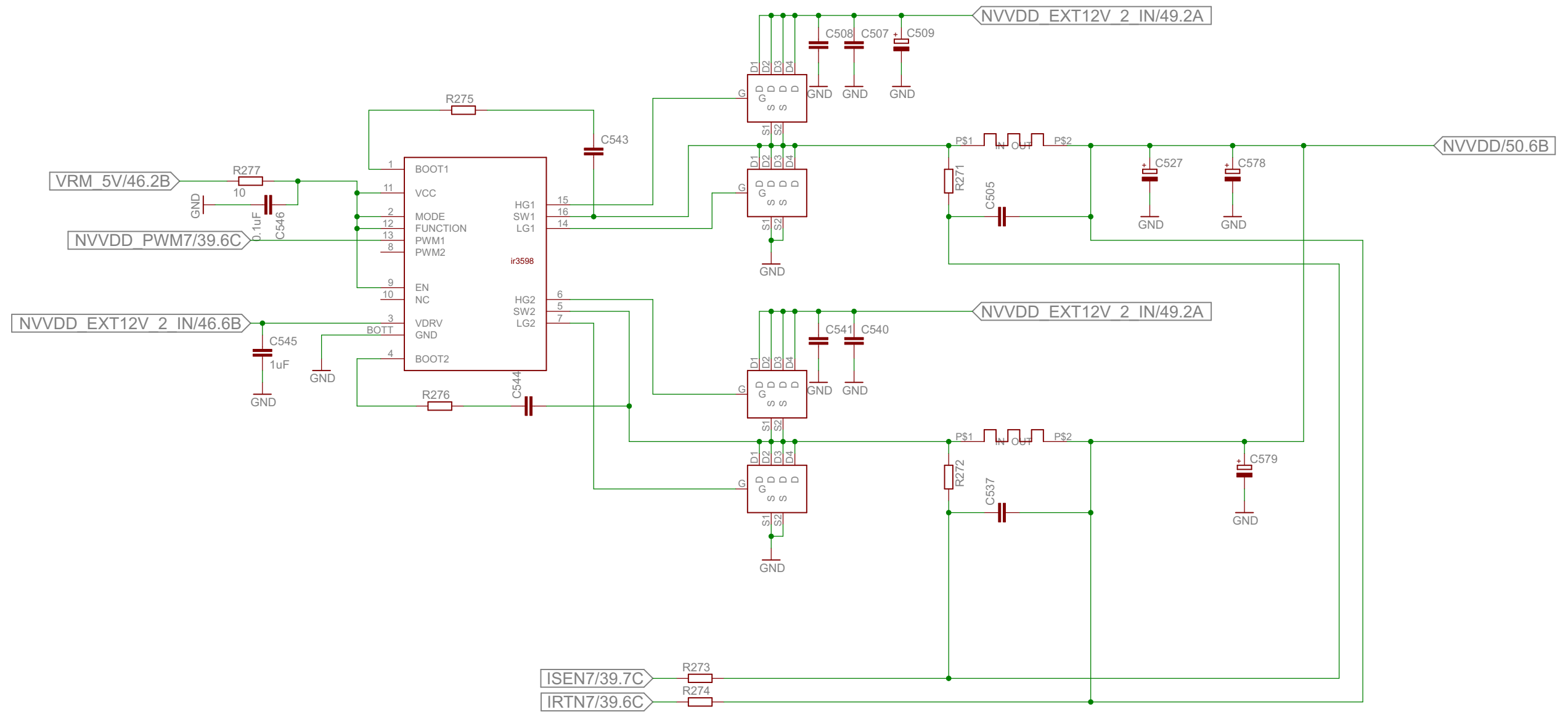


# NVVDD\_PHASE\_11-12

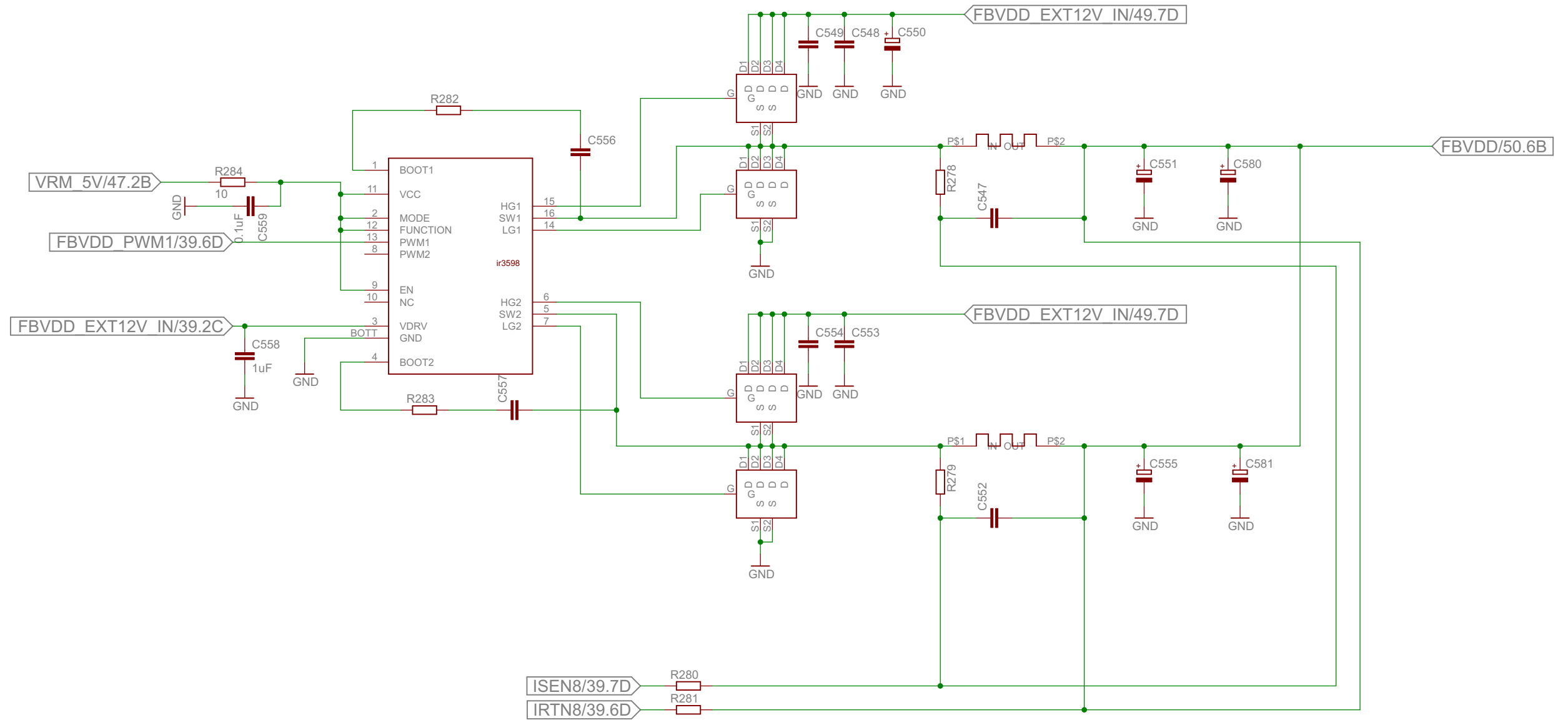


88GTEE
3.3.2014 13:01:41
Sheet: 46/50

# NVVDD\_PHASE\_13-14

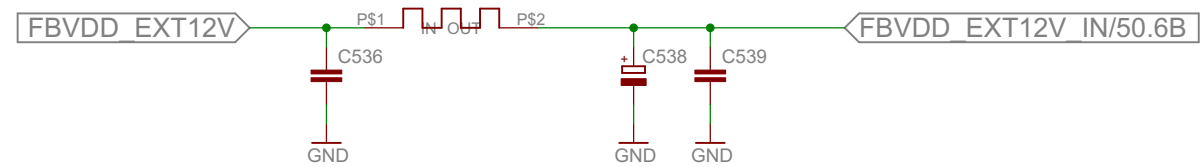
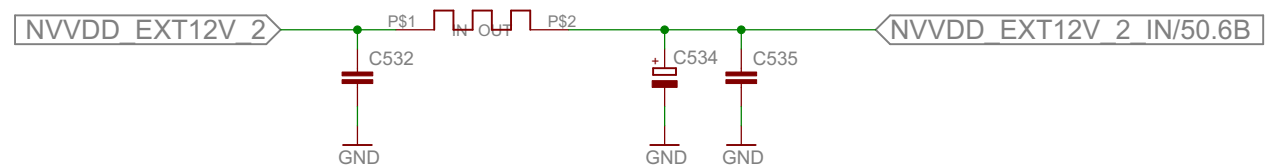
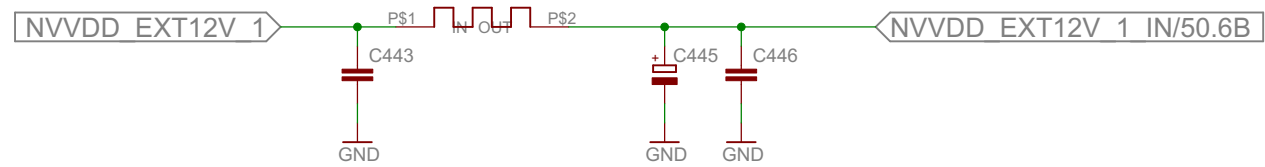
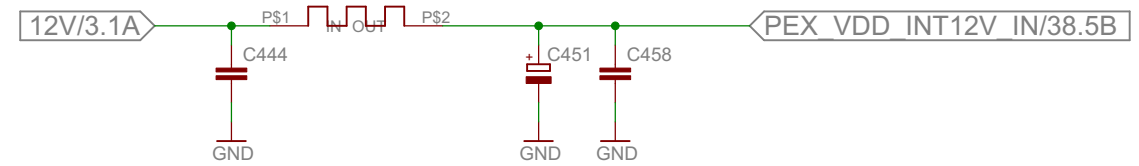
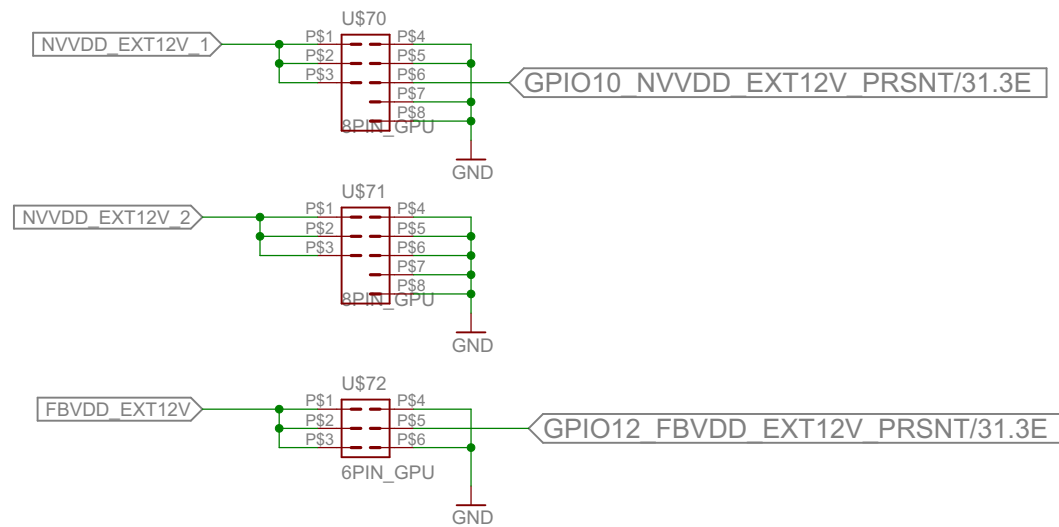
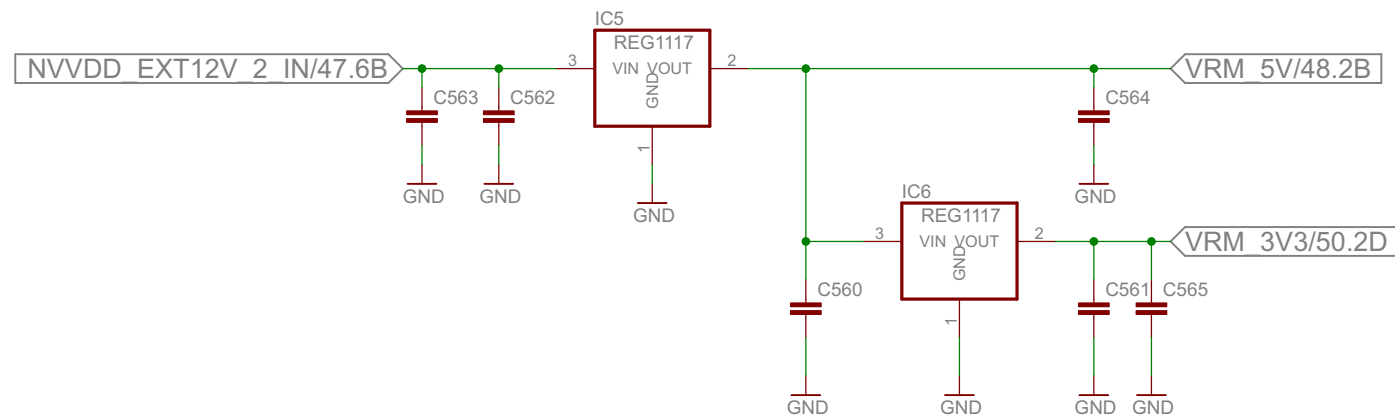


# FBVDD\_PHASE\_1-2



88GTEE  
 3.3.2014 13:01:41  
 Sheet: 48/50

# VRM\_5V/VRM\_3V3/INPUT\_CONN



# MISC

